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(19) **United States**(12) **Patent Application Publication**
Taneda et al.(10) **Pub. No.: US 2014/0332797 A1**(43) **Pub. Date: Nov. 13, 2014**(54) **ELECTRO LUMINESCENT DISPLAY PANEL
AND ELECTRONIC APPARATUS**(30) **Foreign Application Priority Data**

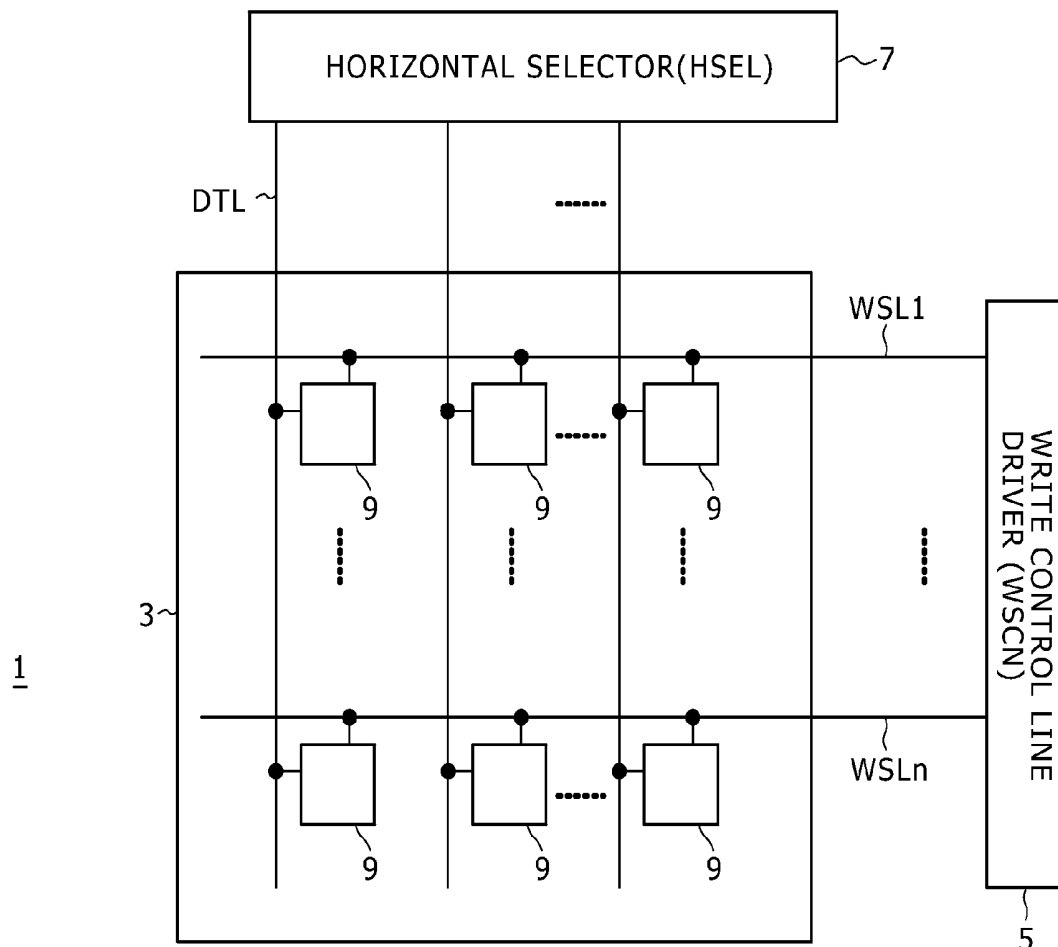
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H01L 27/32 (2006.01)
H01L 51/50 (2006.01)(73) Assignee: **Sony Corporation**, Tokyo (JP)(52) **U.S. Cl.**
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(2013.01); **H01L 51/5012** (2013.01)
USPC **257/40**(21) Appl. No.: **14/445,104**(57) **ABSTRACT**(22) Filed: **Jul. 29, 2014**

An EL display panel having a pixel structure corresponding to an active-matrix drive system, the EL display panel including a current supply line configured to be connected to a plurality of pixel circuits in common, line width of an intersection part of the current supply line with a signal line being smaller than line width of the other part of the current supply line.

Related U.S. Application Data

(63) Continuation of application No. 12/292,339, filed on Nov. 17, 2008.



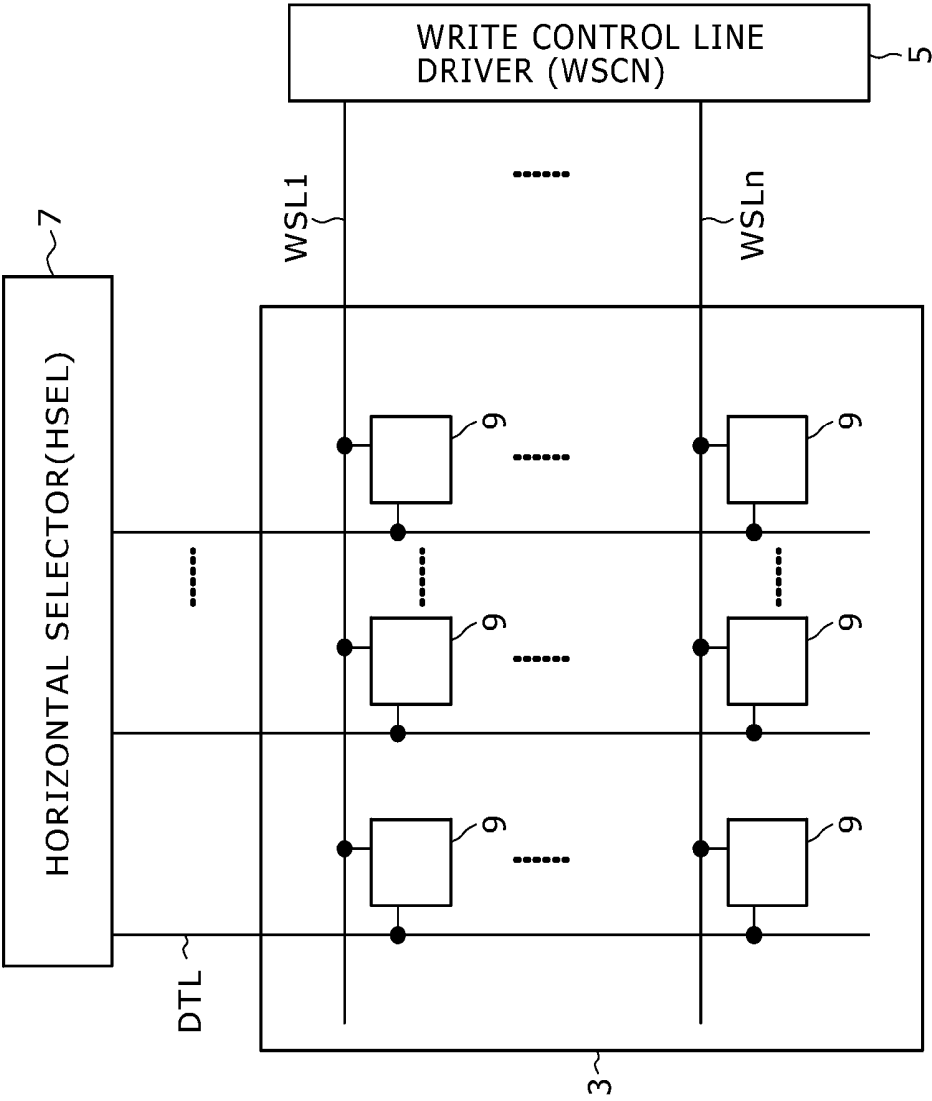


FIG. 1

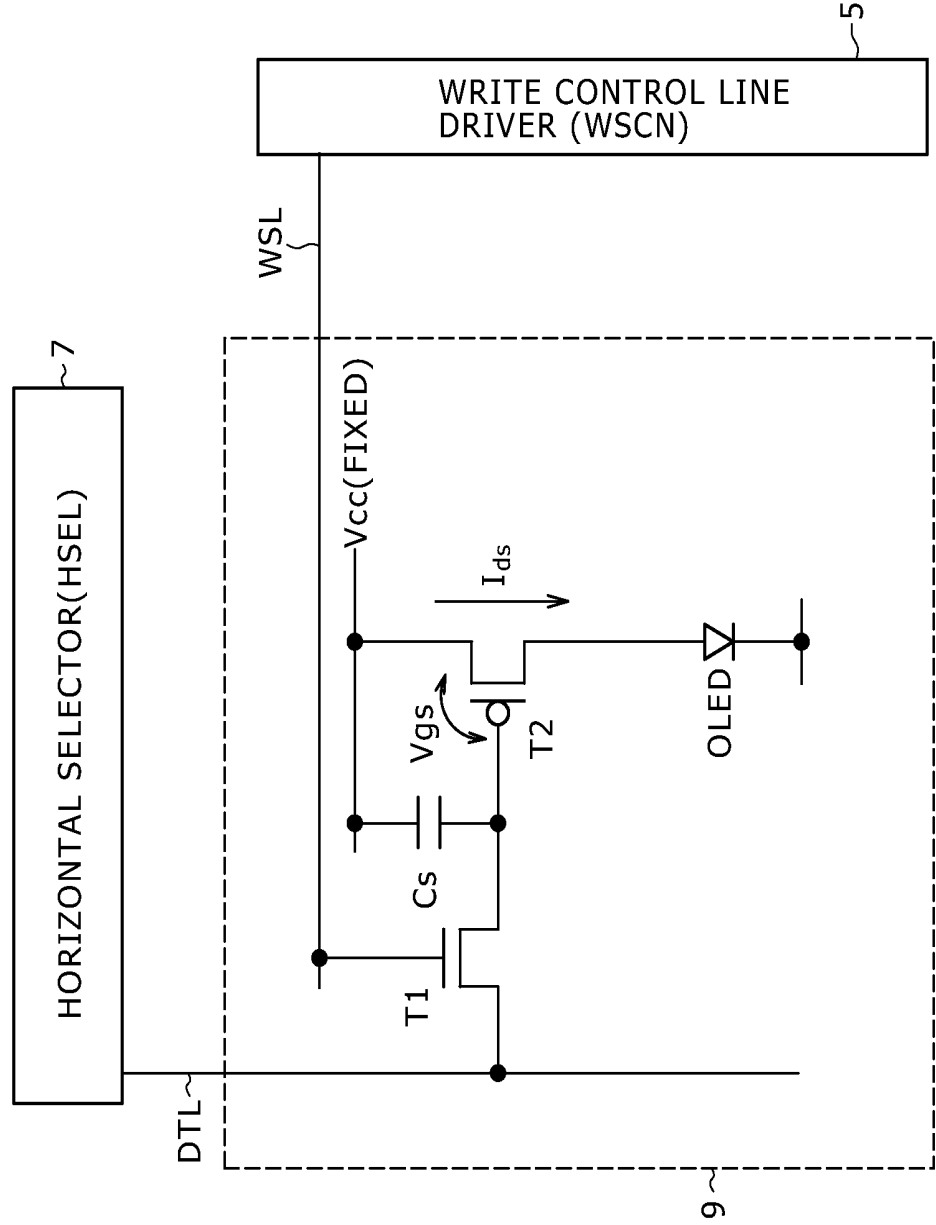
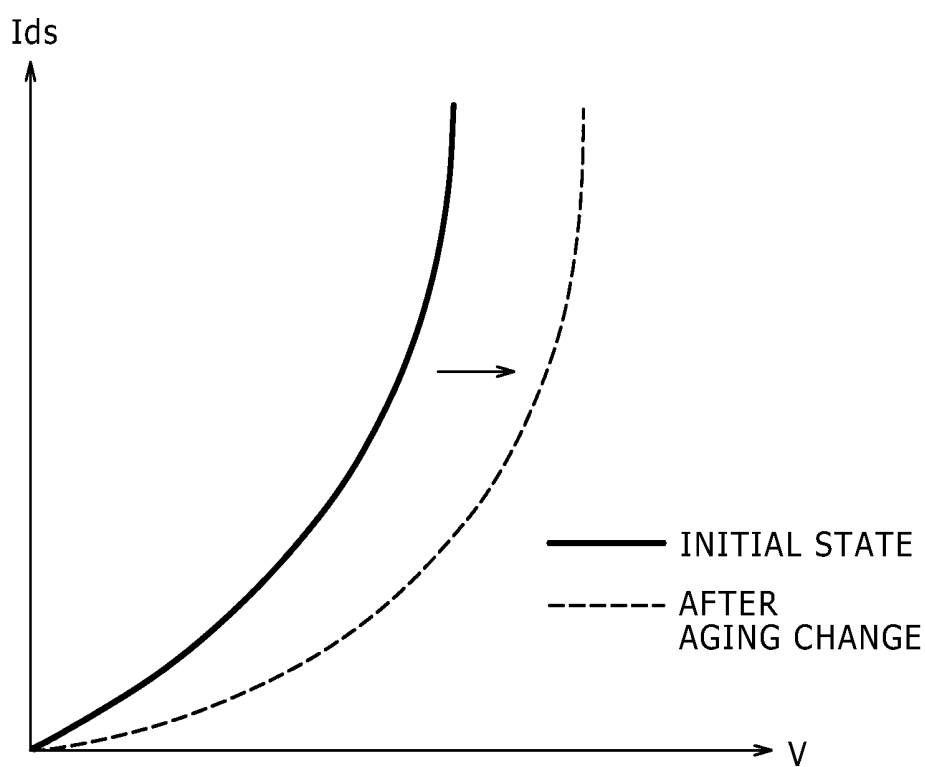


FIG. 2

FIG. 3



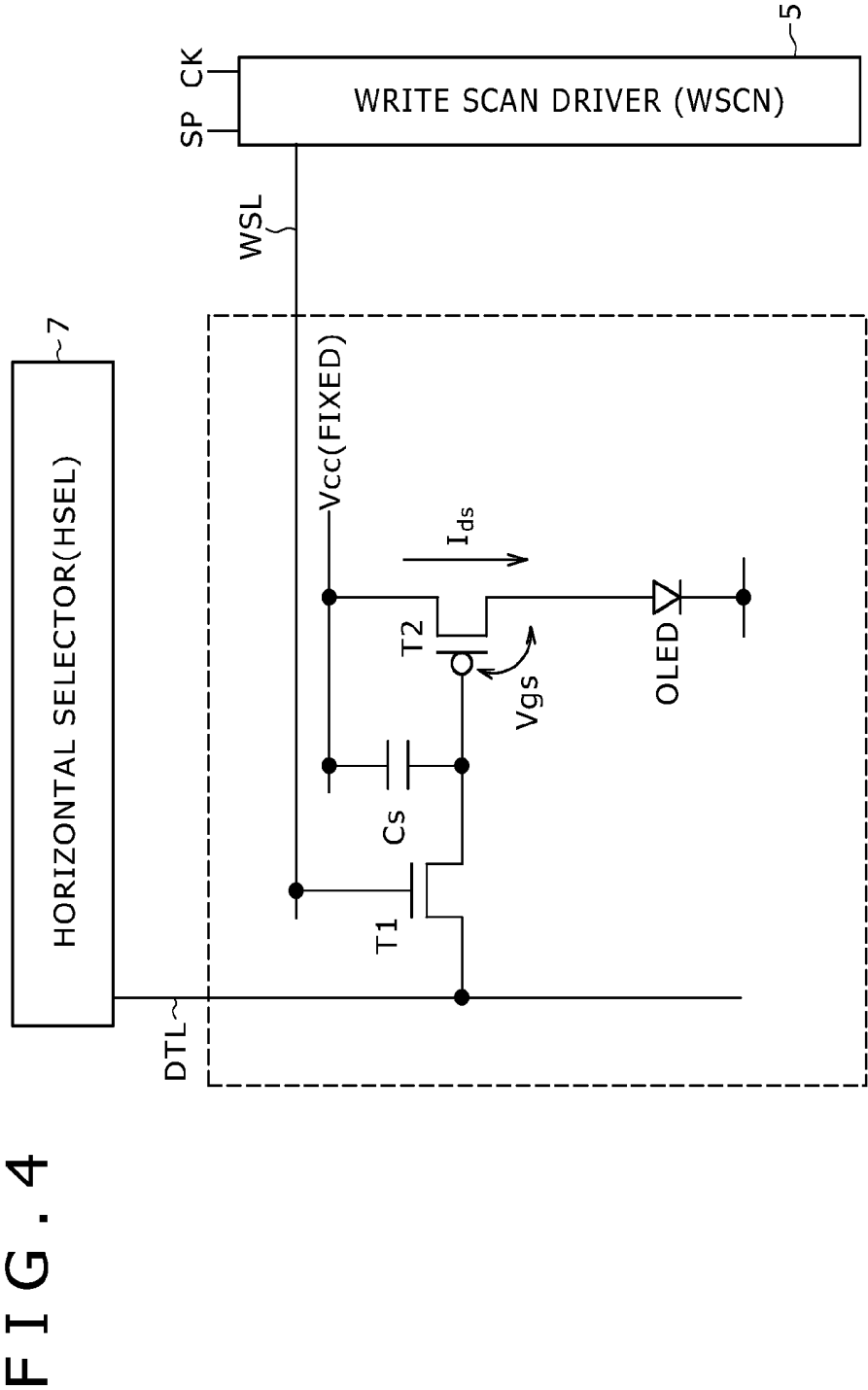
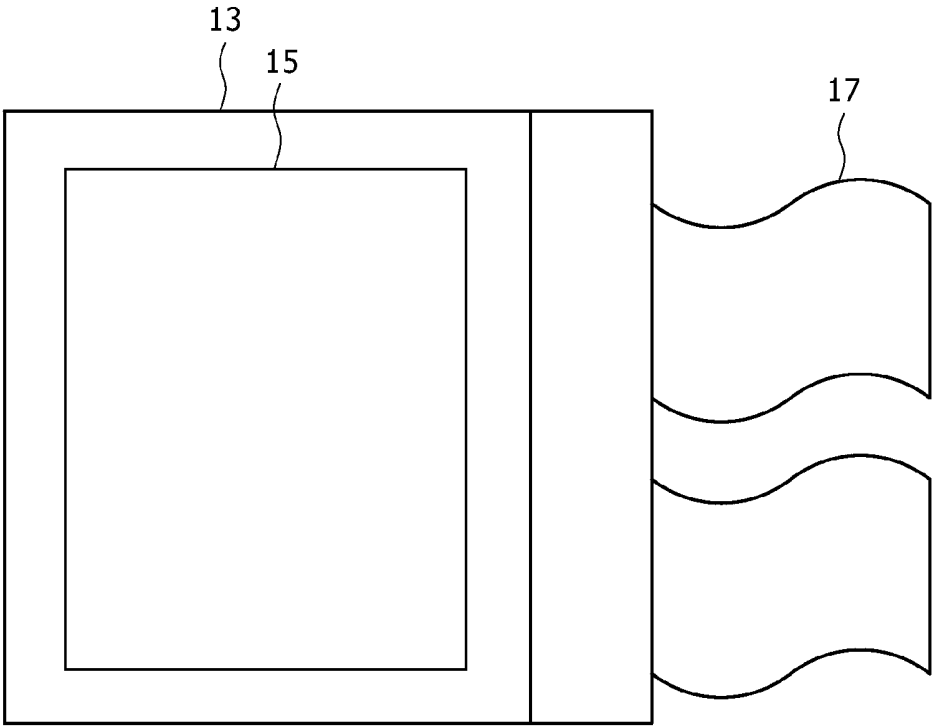
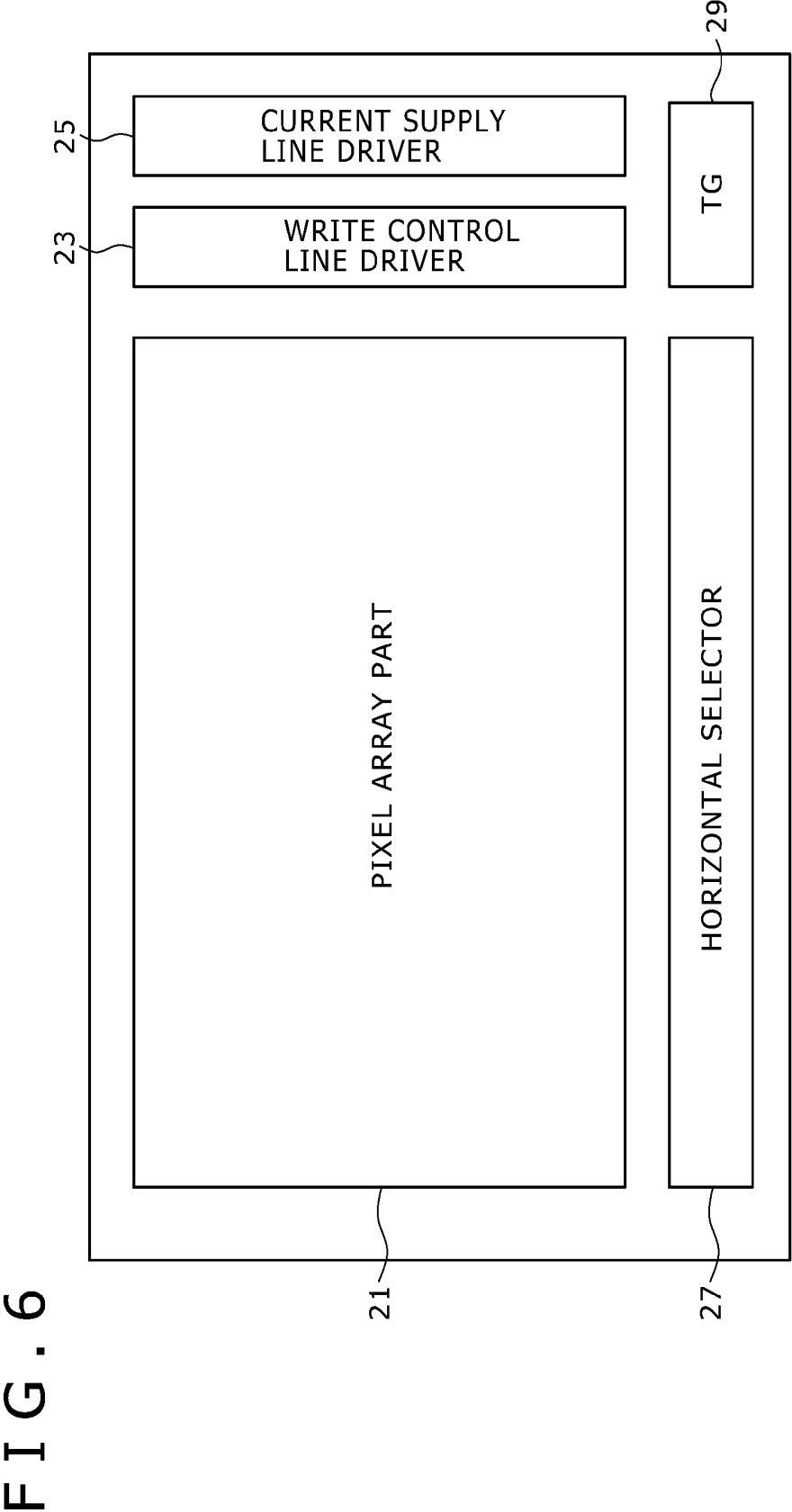


FIG. 5





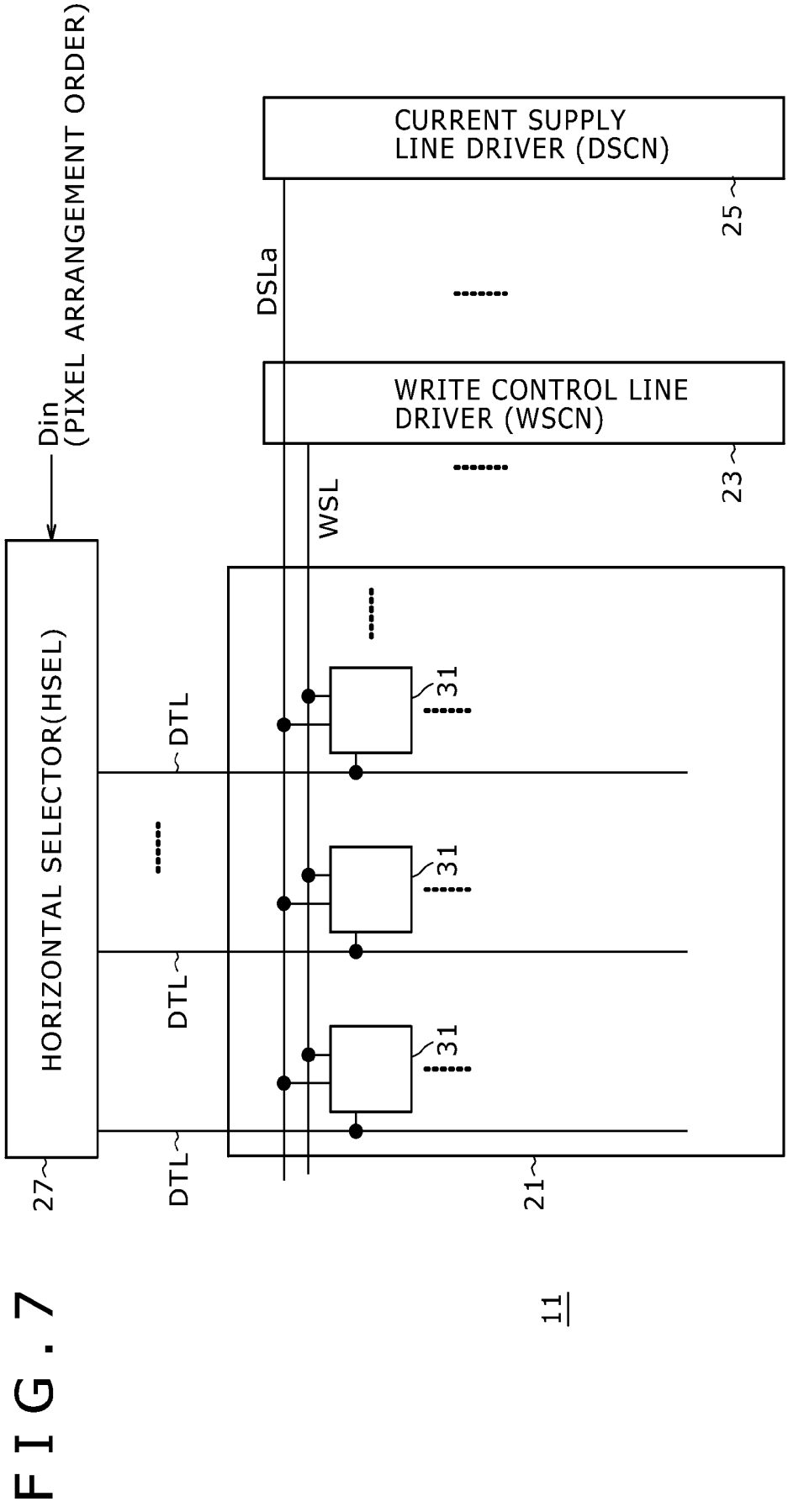
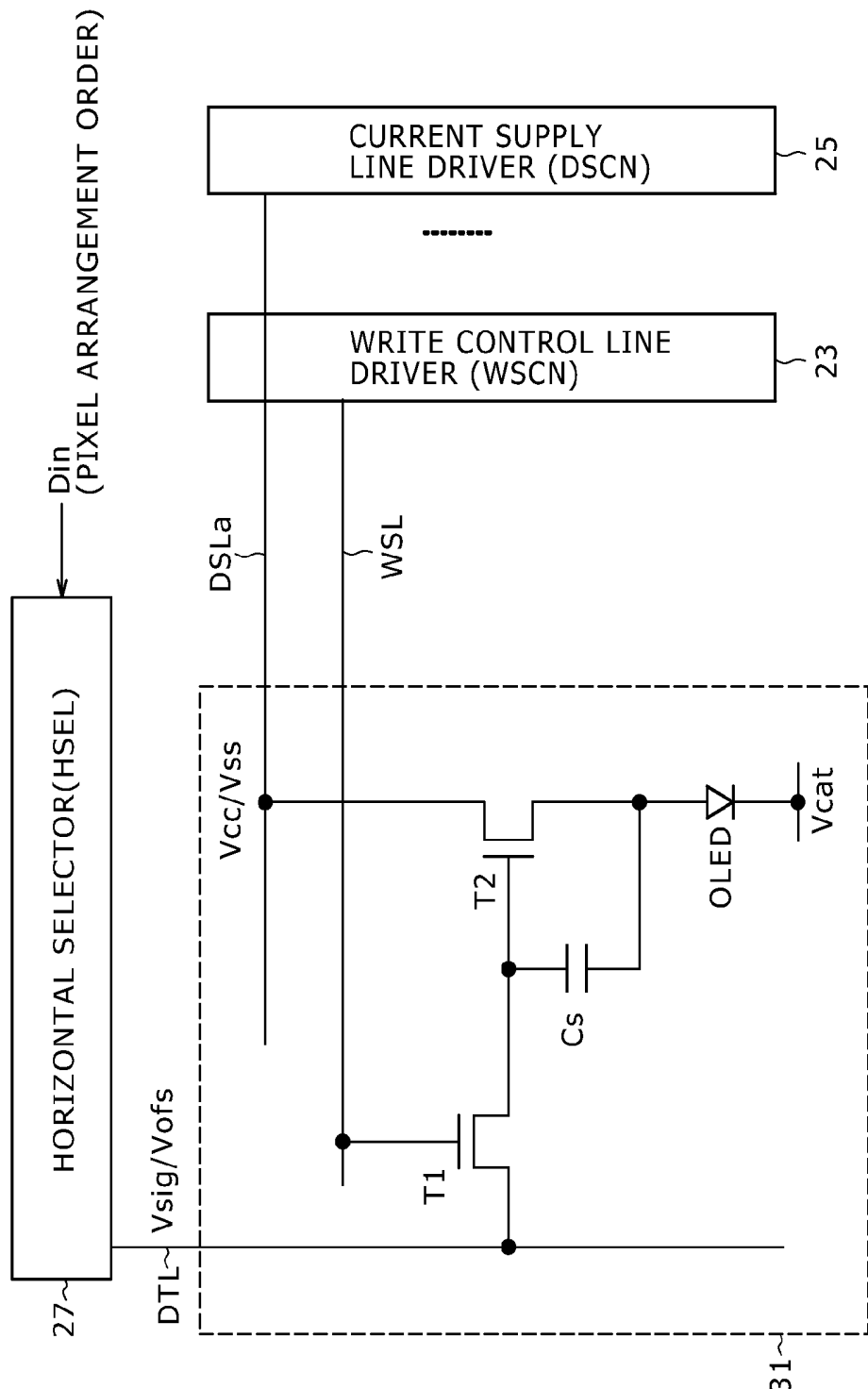


FIG. 8



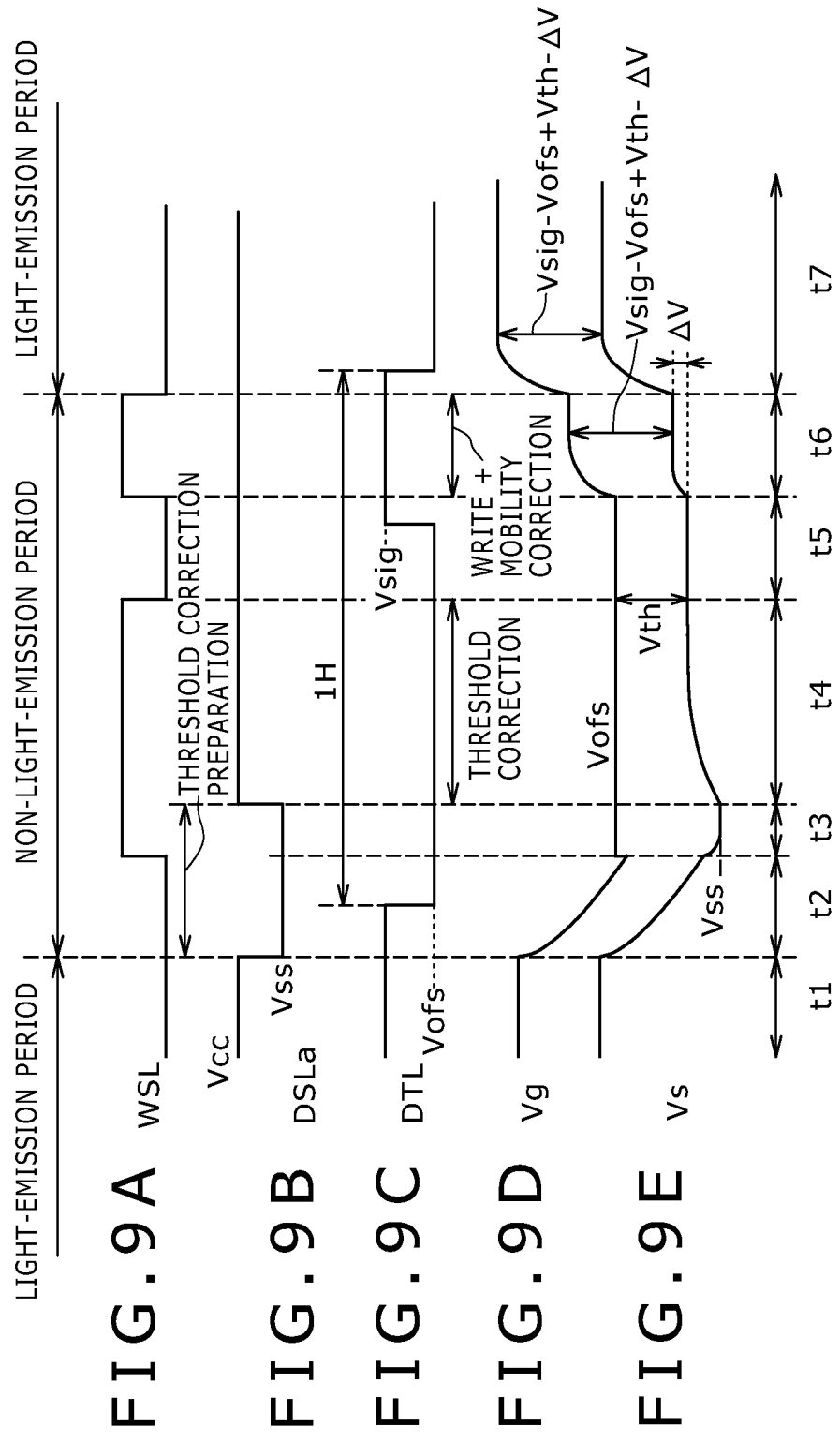


FIG. 10

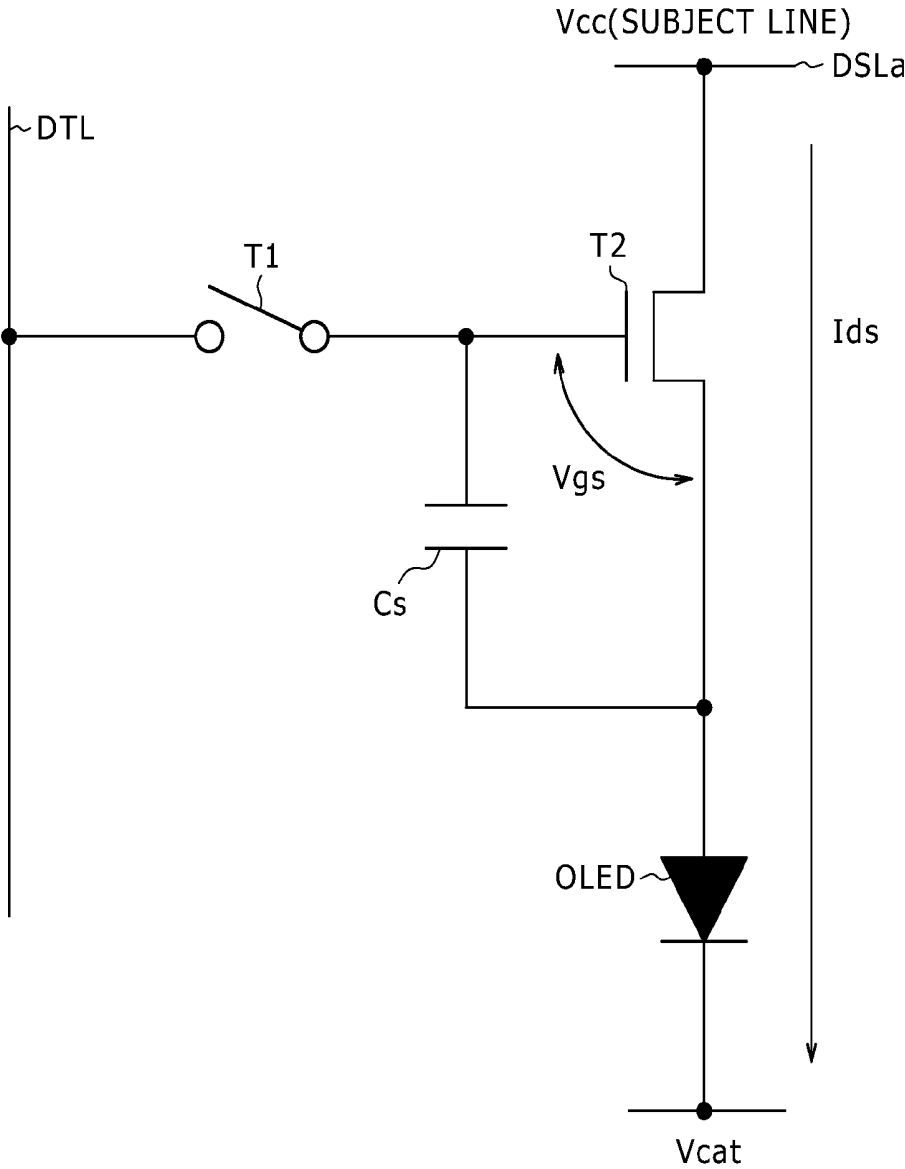


FIG. 11

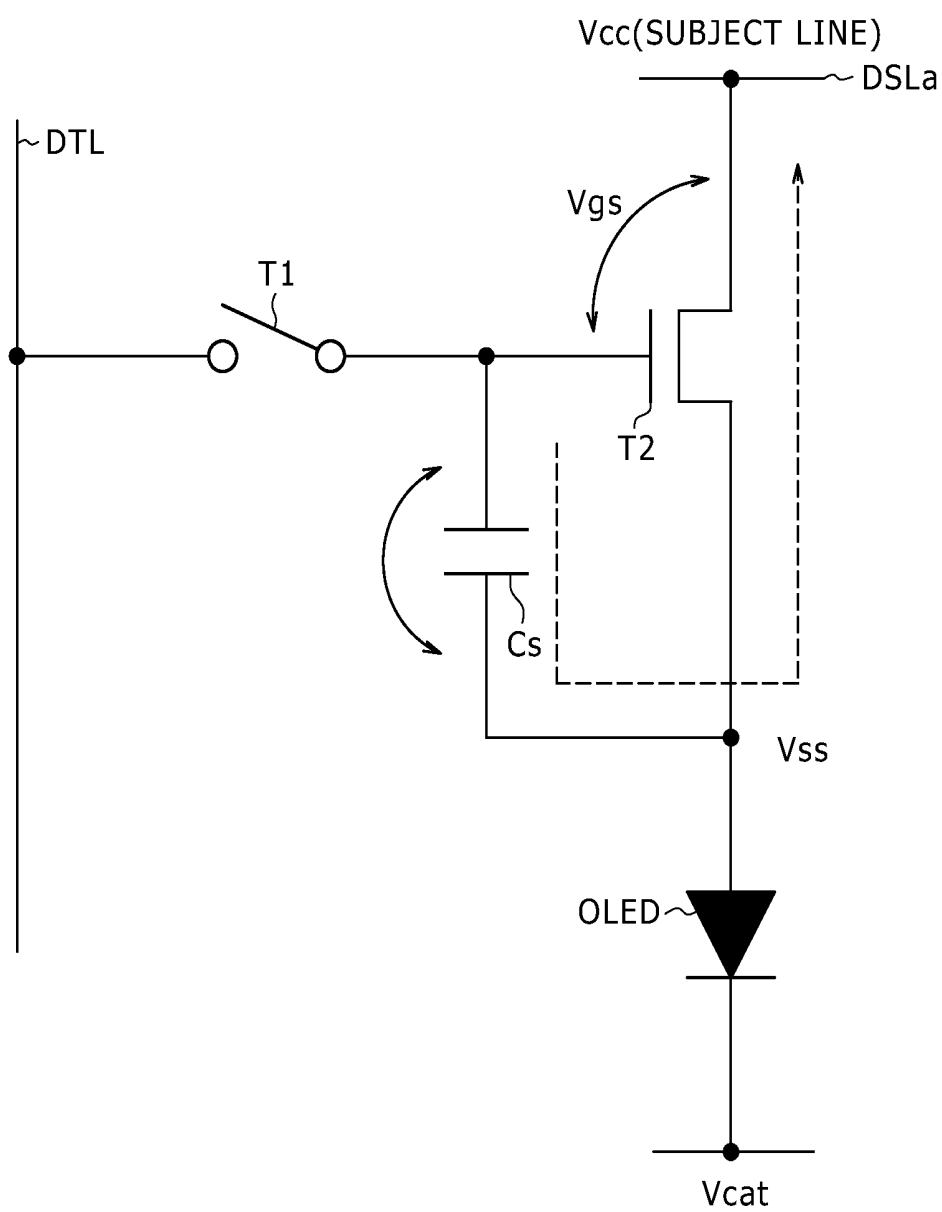


FIG. 12

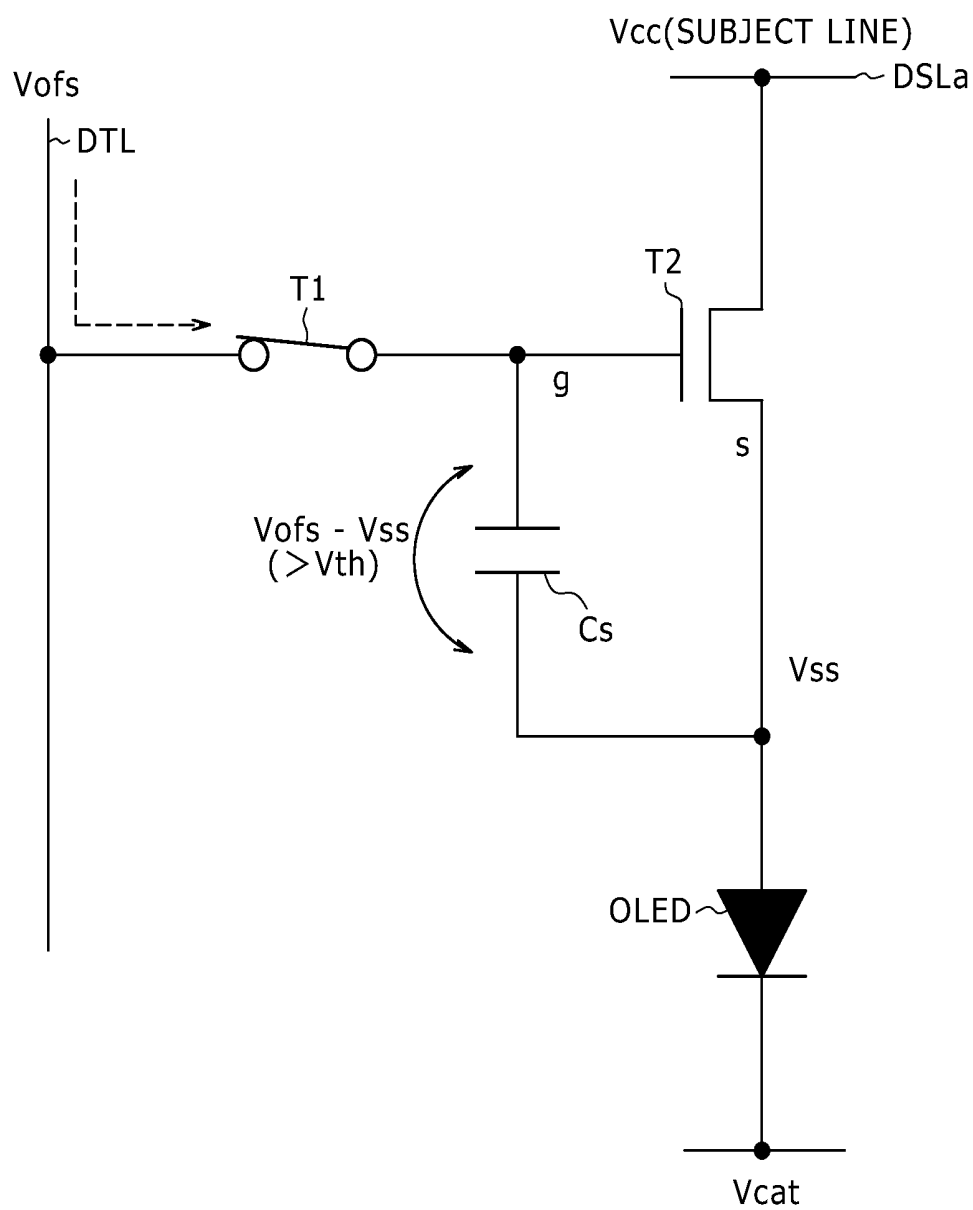


FIG. 13

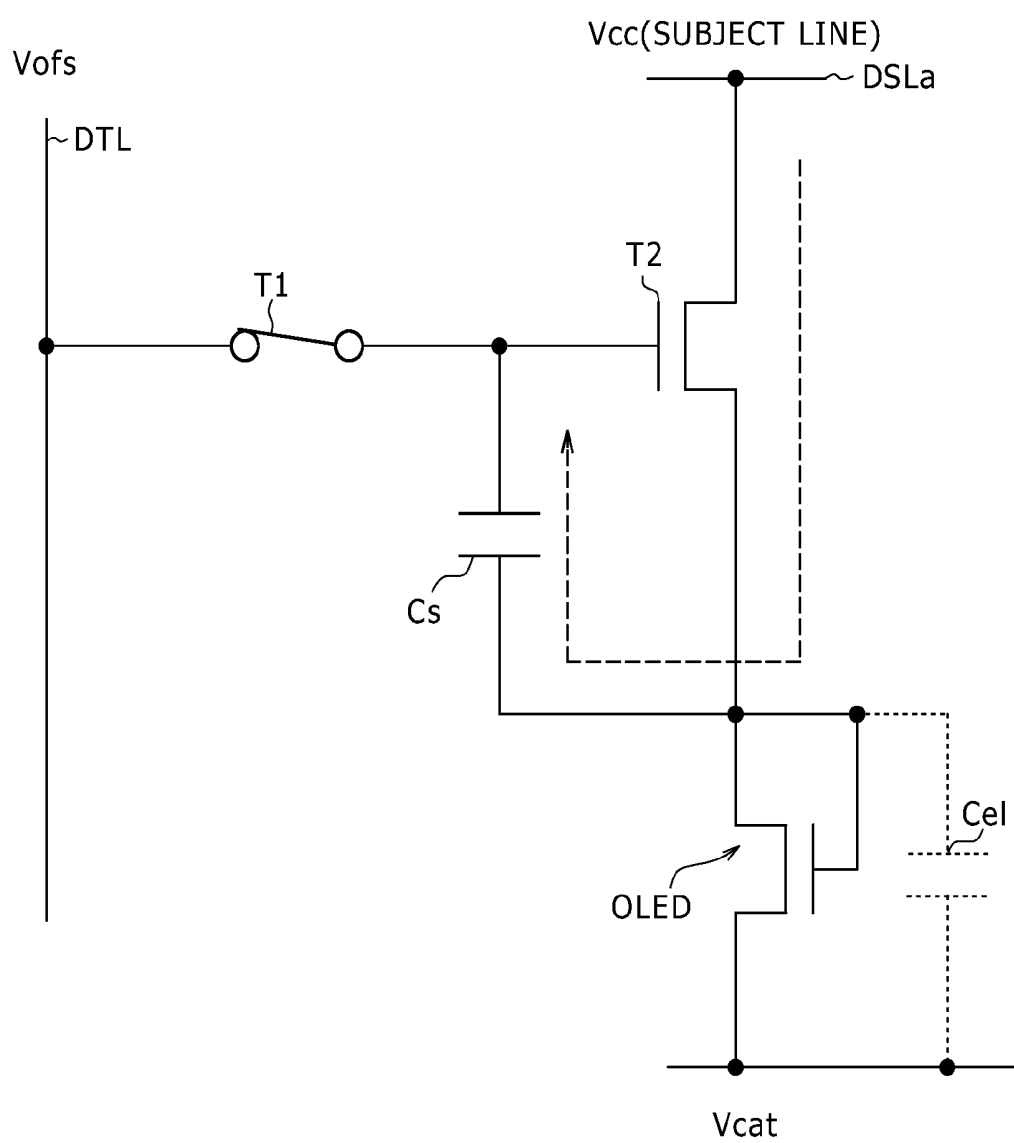


FIG. 14

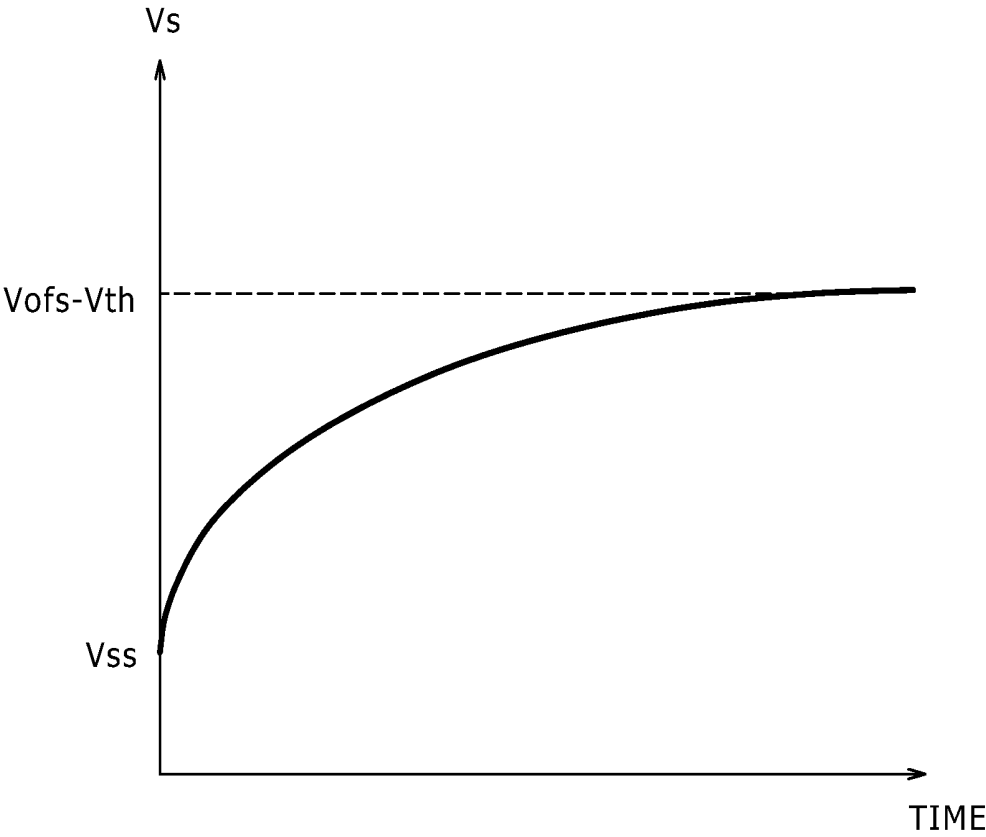


FIG. 15

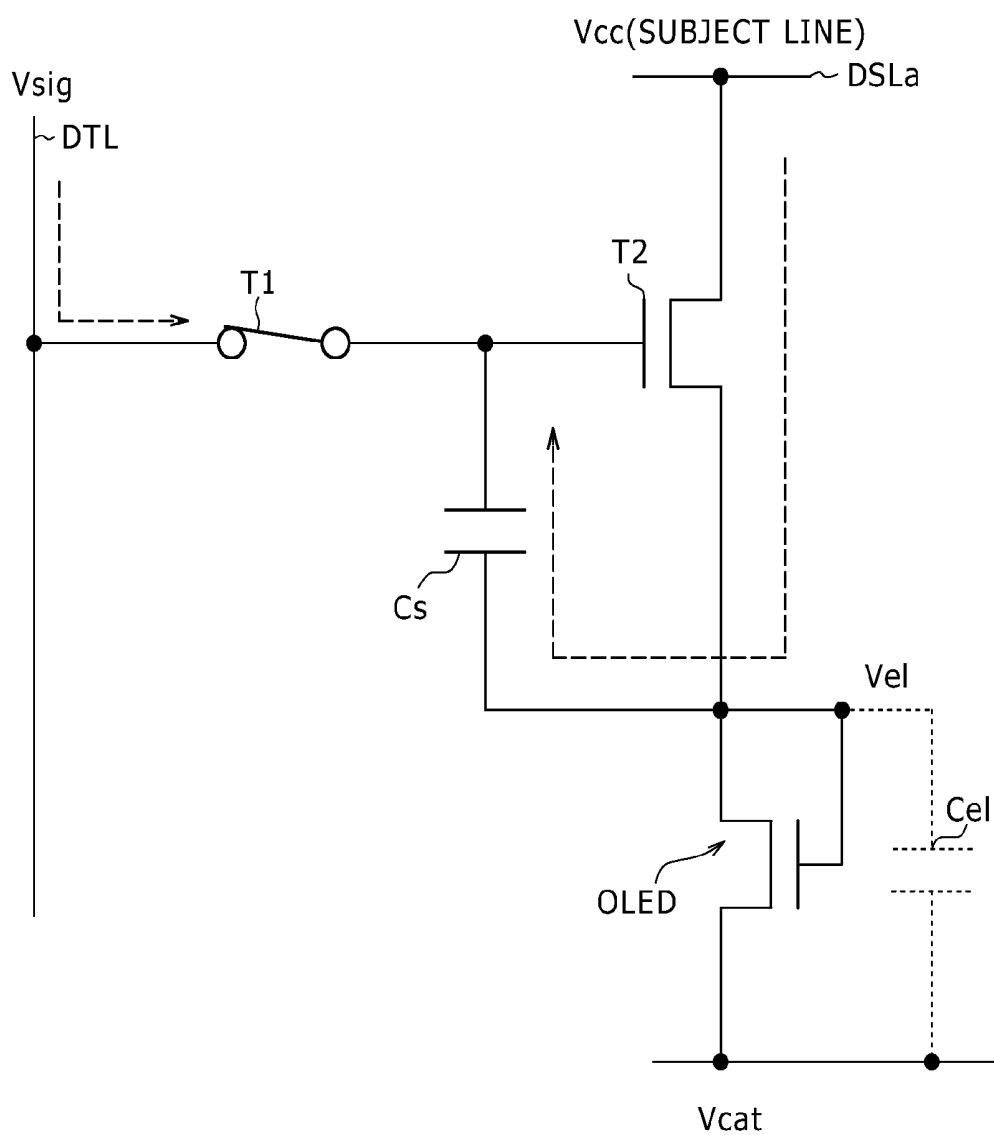


FIG. 16

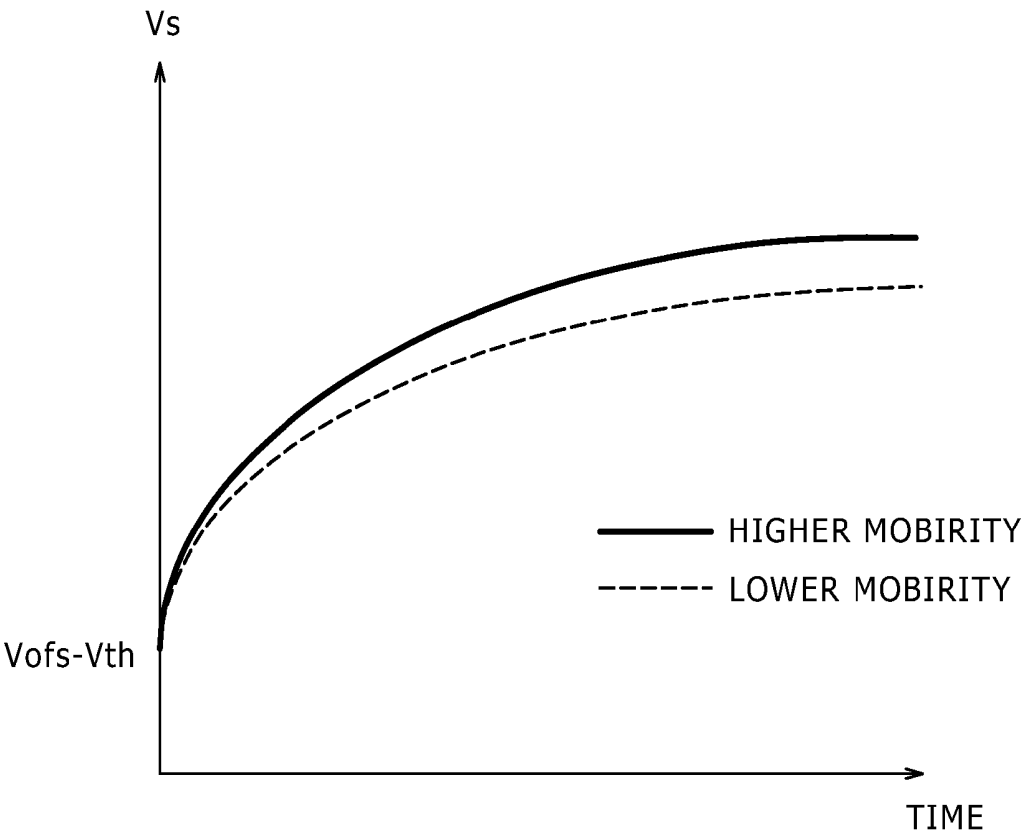
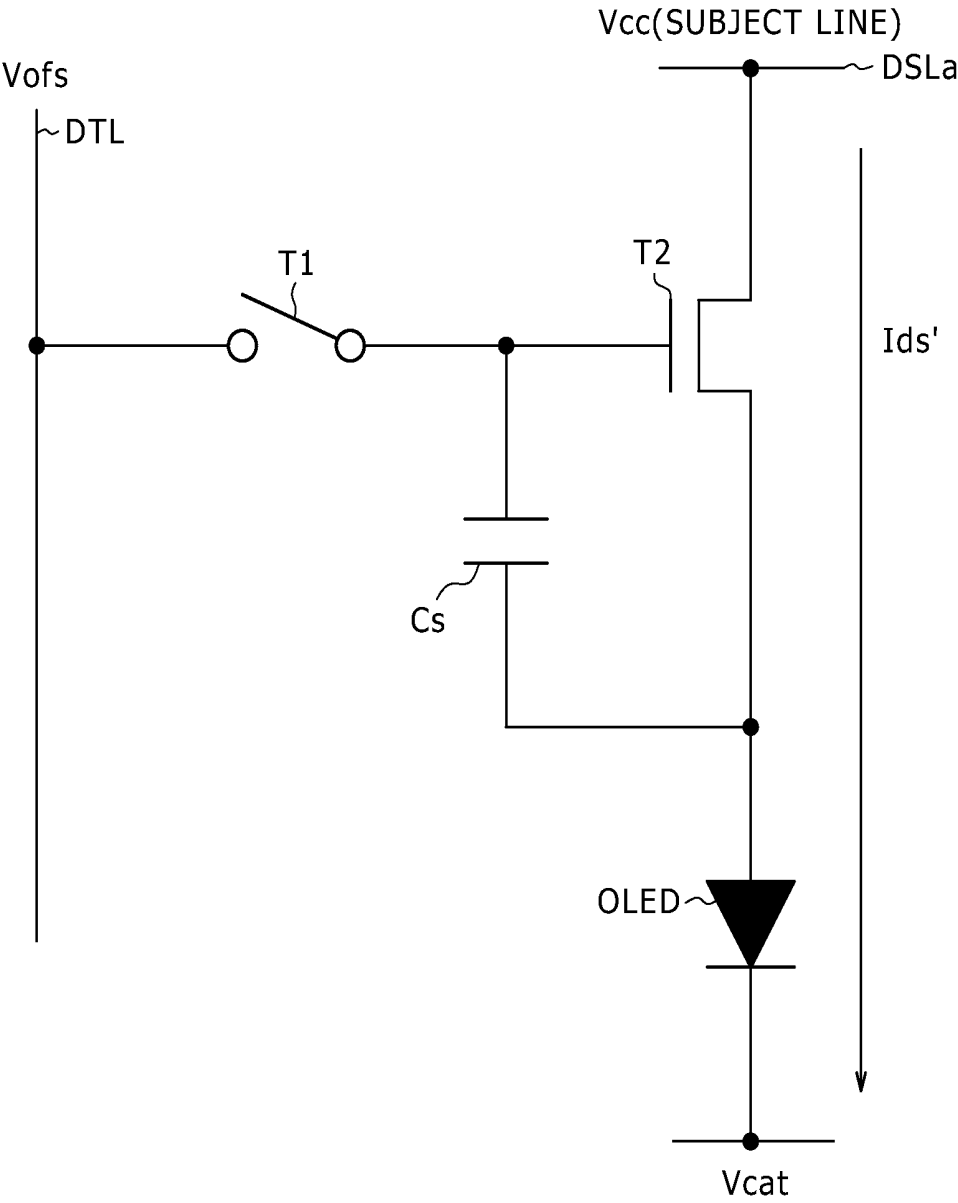


FIG. 17



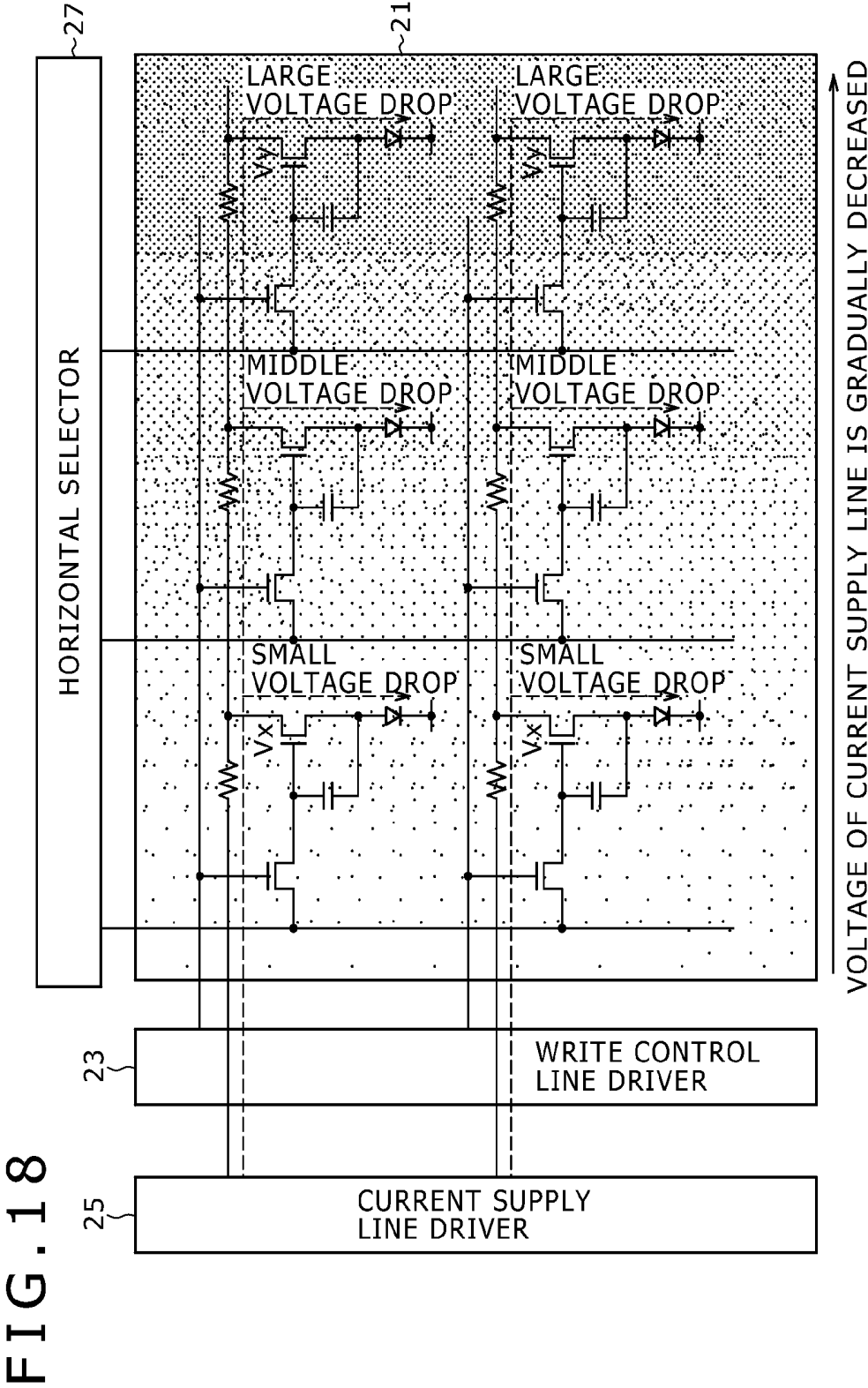


FIG. 19

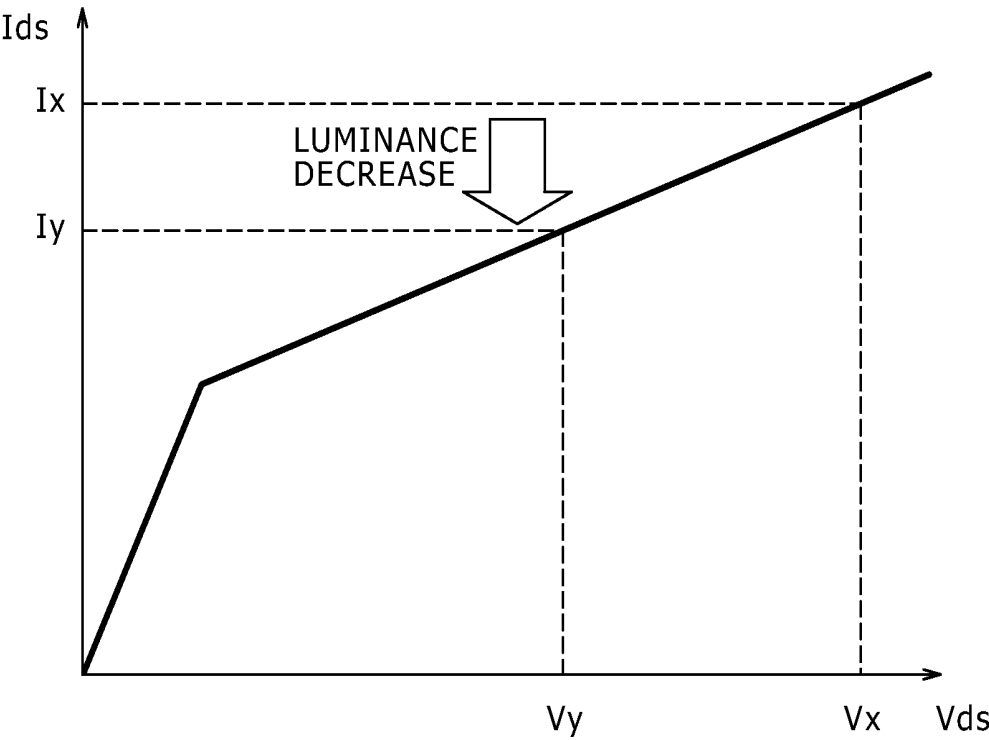


FIG. 20A

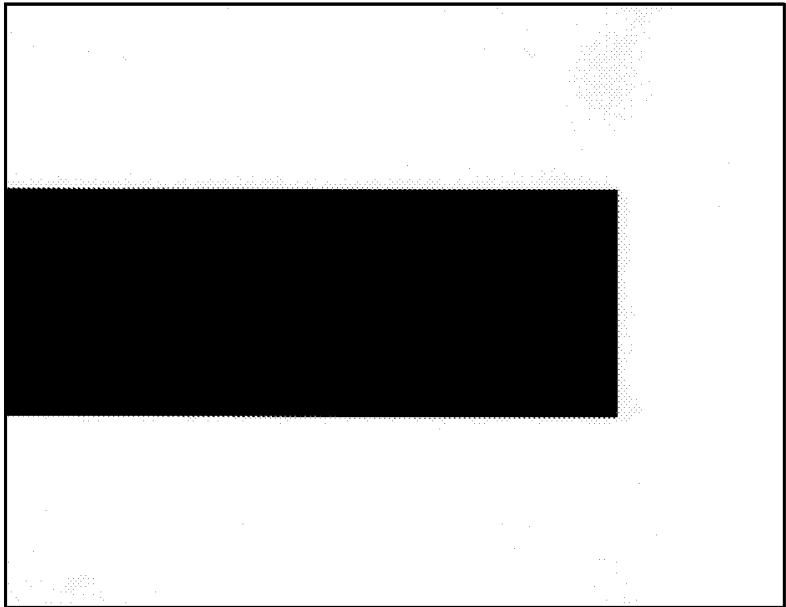
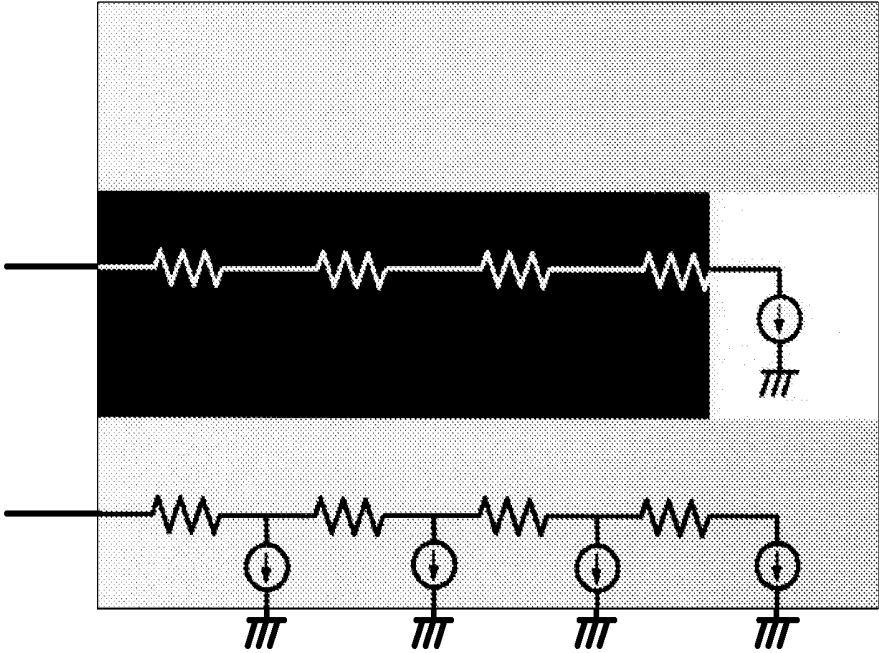


FIG. 20B



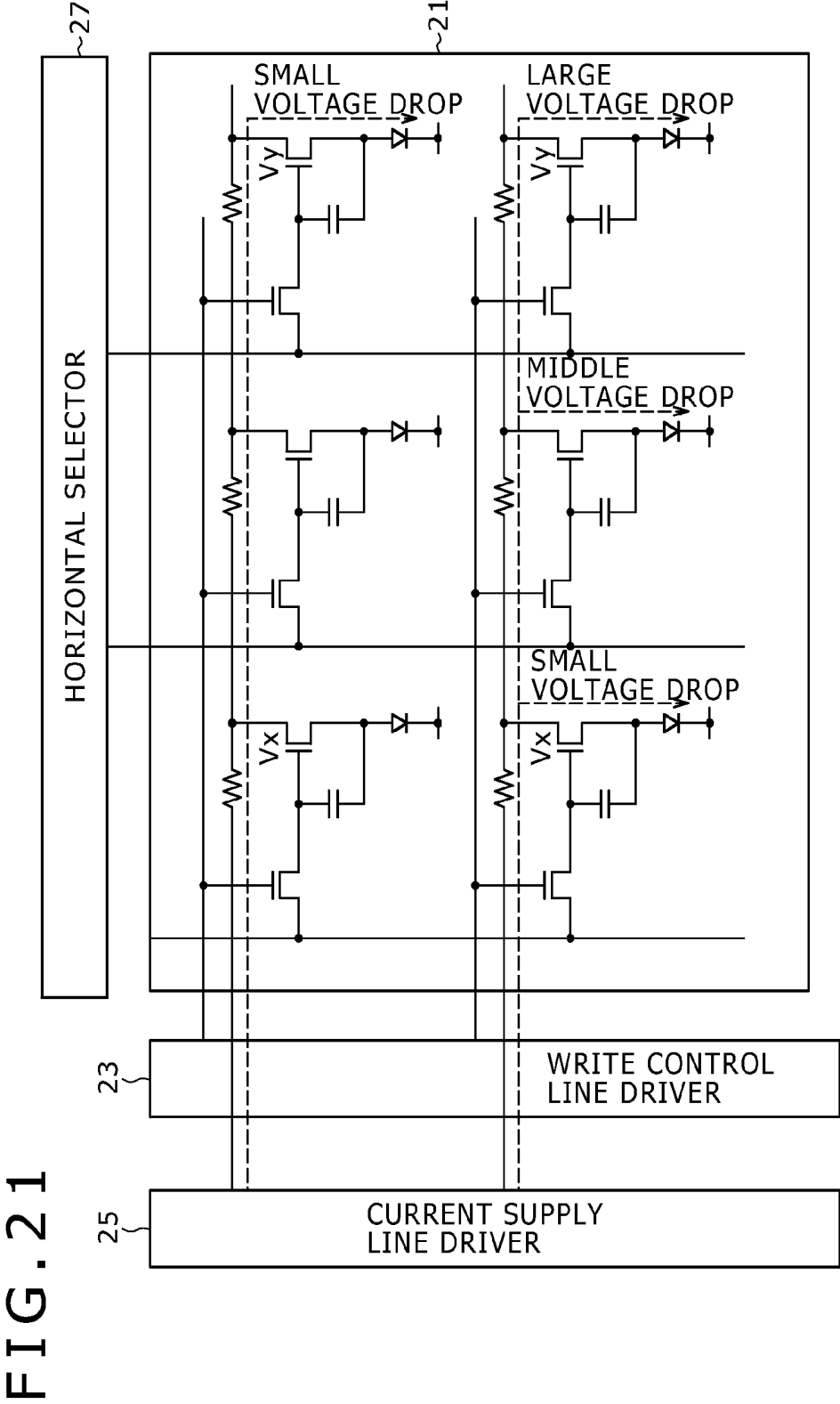
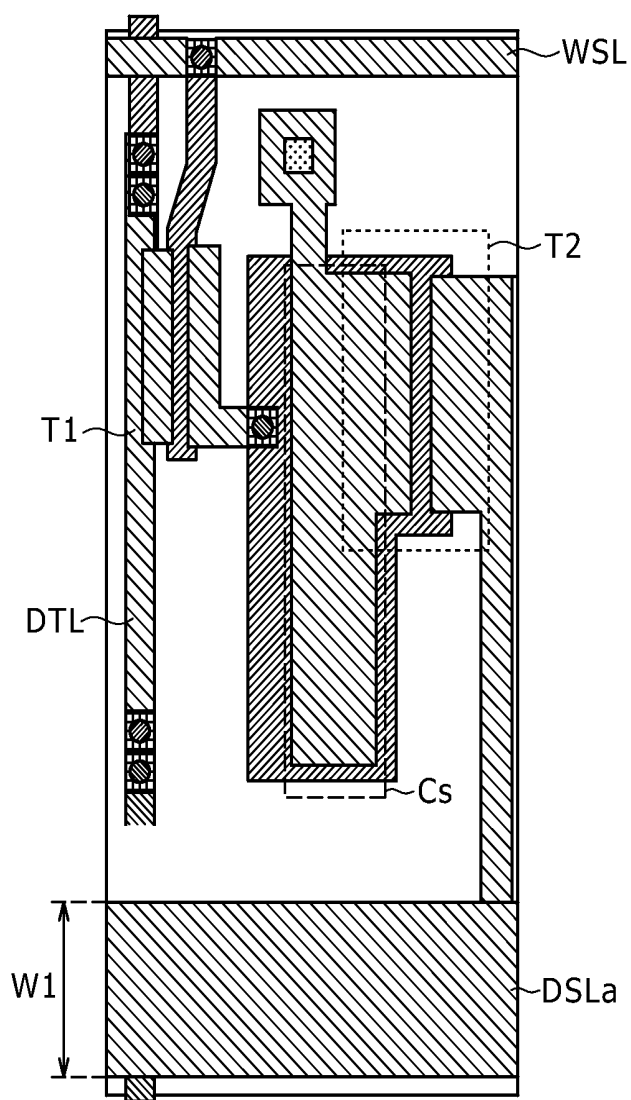


FIG. 22



 FIRST METAL LAYER

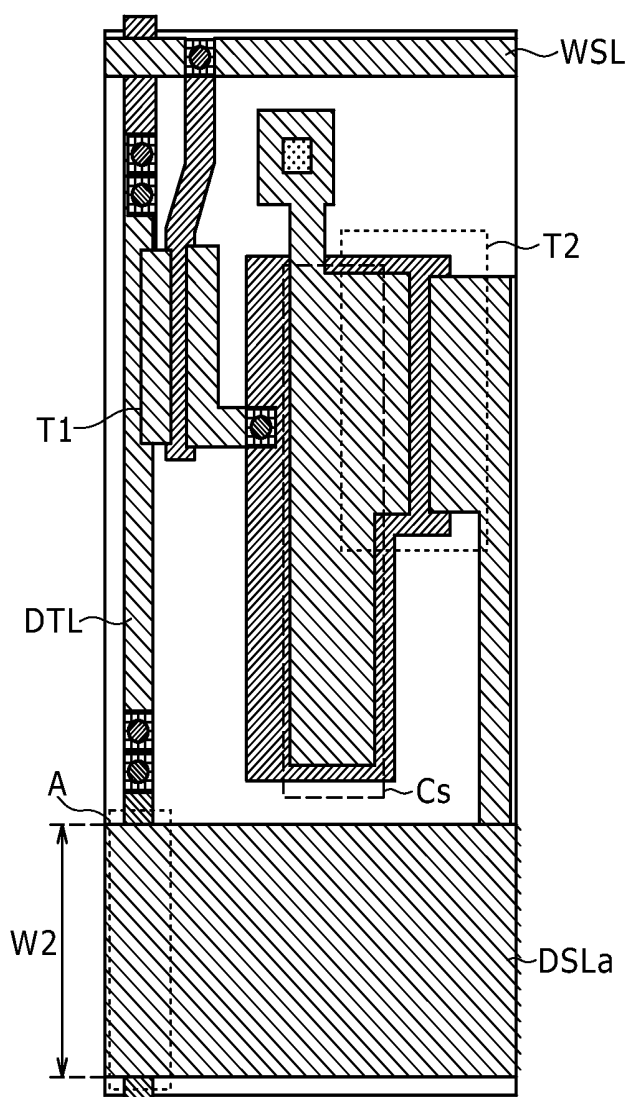
 CONTACT BETWEEN FIRST METAL LAYER AND SECOND METAL LAYER

 SECOND METAL LAYER

 CONTACT BETWEEN SECOND METAL LAYER AND THIRD METAL LAYER

 FORMATION AREA OF HOLD CAPACITOR

FIG. 23



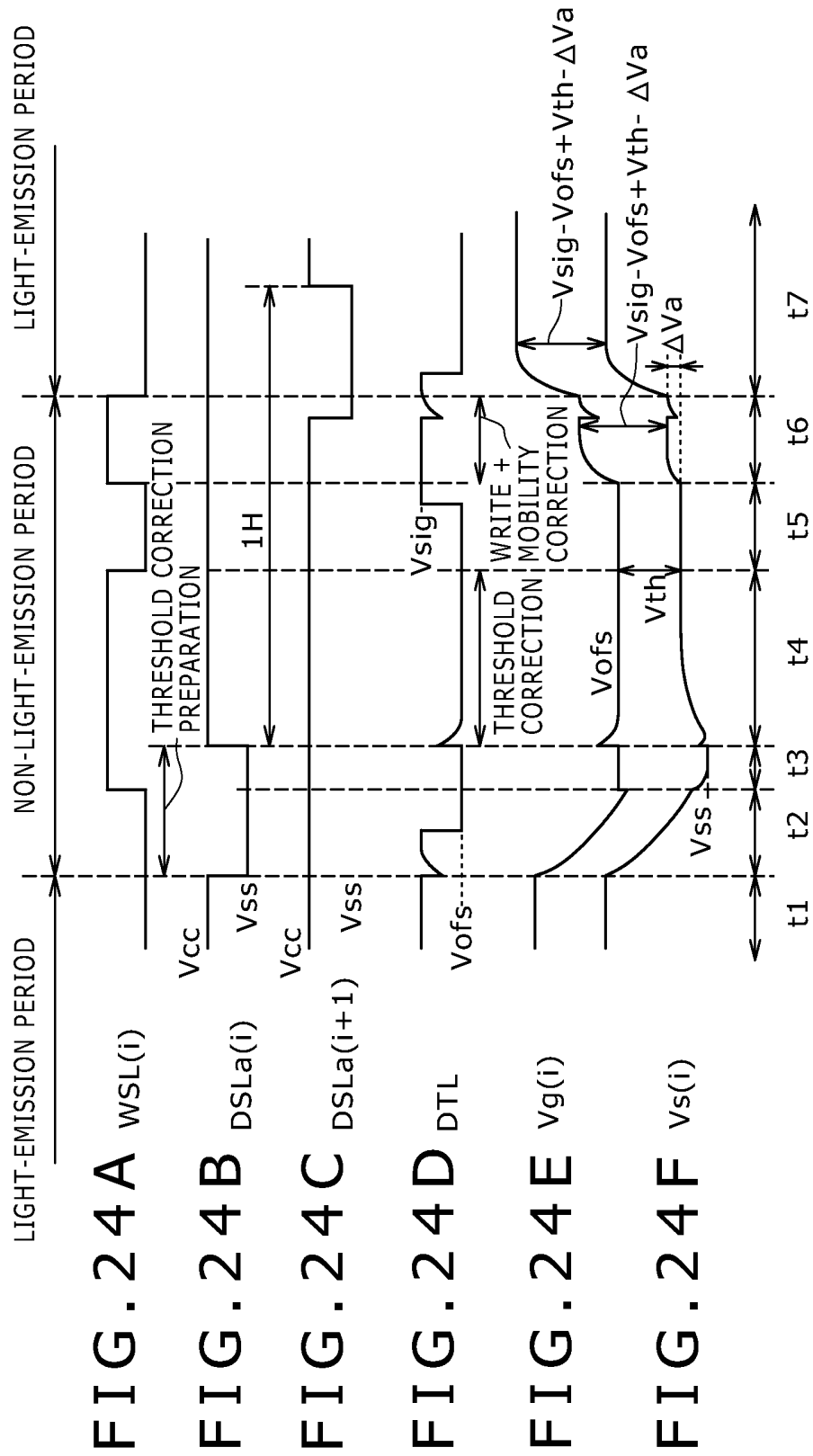
 FIRST METAL LAYER

 SECOND METAL LAYER

 CONTACT BETWEEN FIRST METAL LAYER AND SECOND METAL LAYER

 CONTACT BETWEEN SECOND METAL LAYER AND THIRD METAL LAYER

 FORMATION AREA OF HOLD CAPACITOR



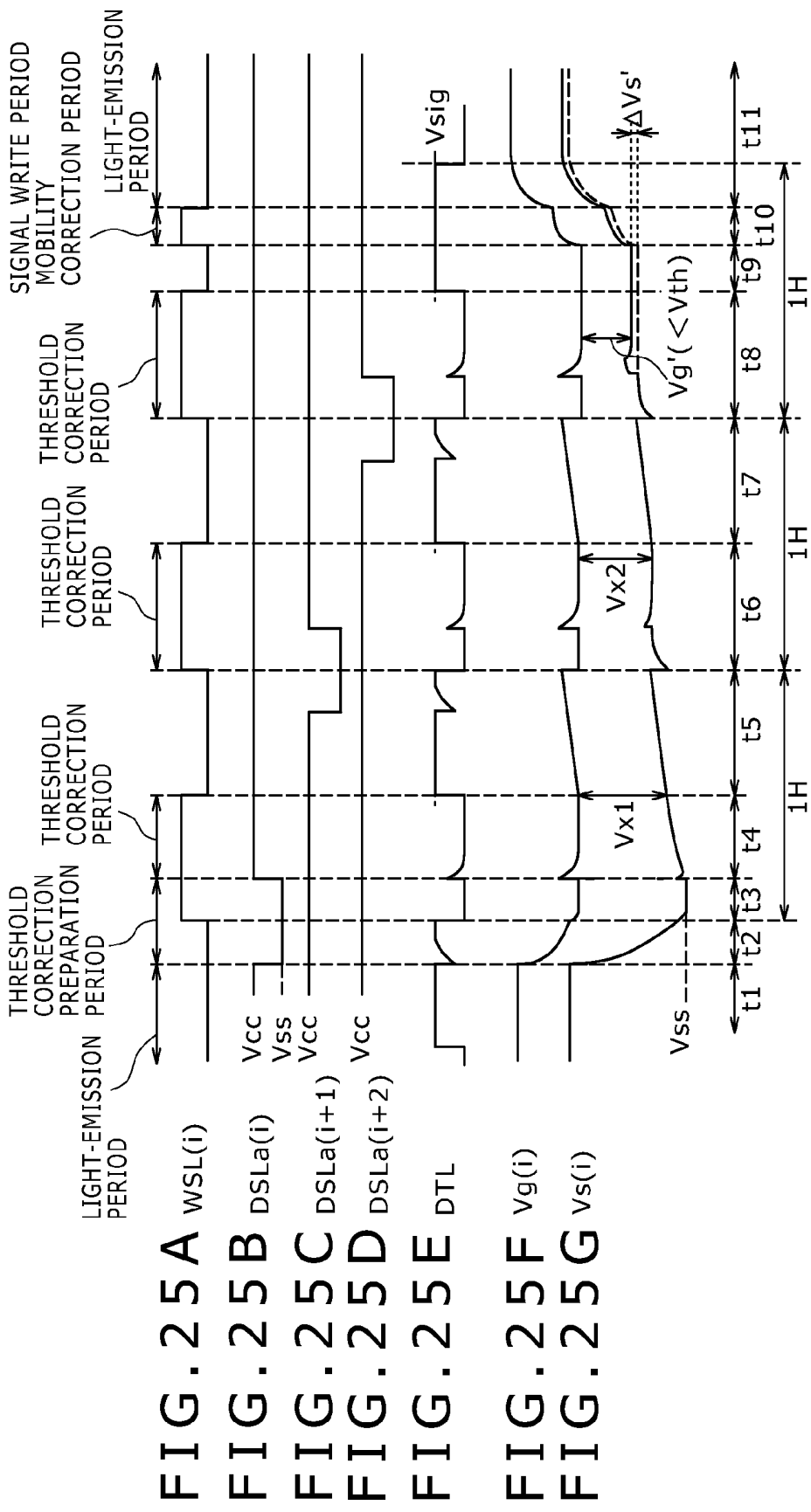


FIG. 26A

$V_{gs} = V_{th}$

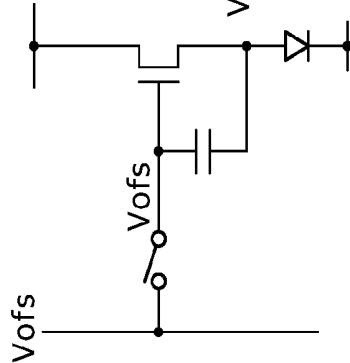


FIG. 26B

$V_{gs} > V_{th}$

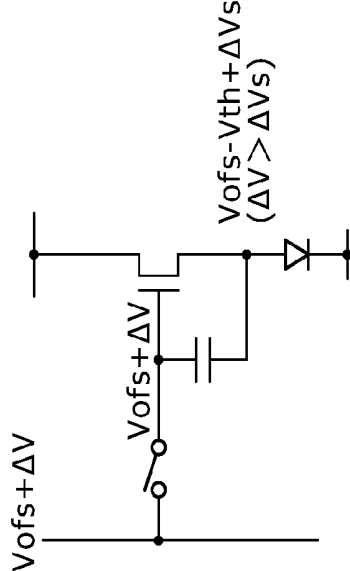


FIG. 26C

$V_{gs} > V_{th}$

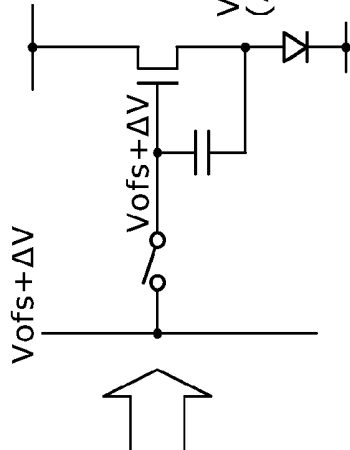


FIG. 26D

$V_{gs} < V_{th}$

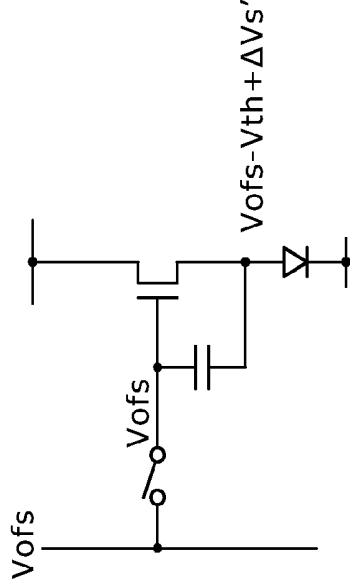
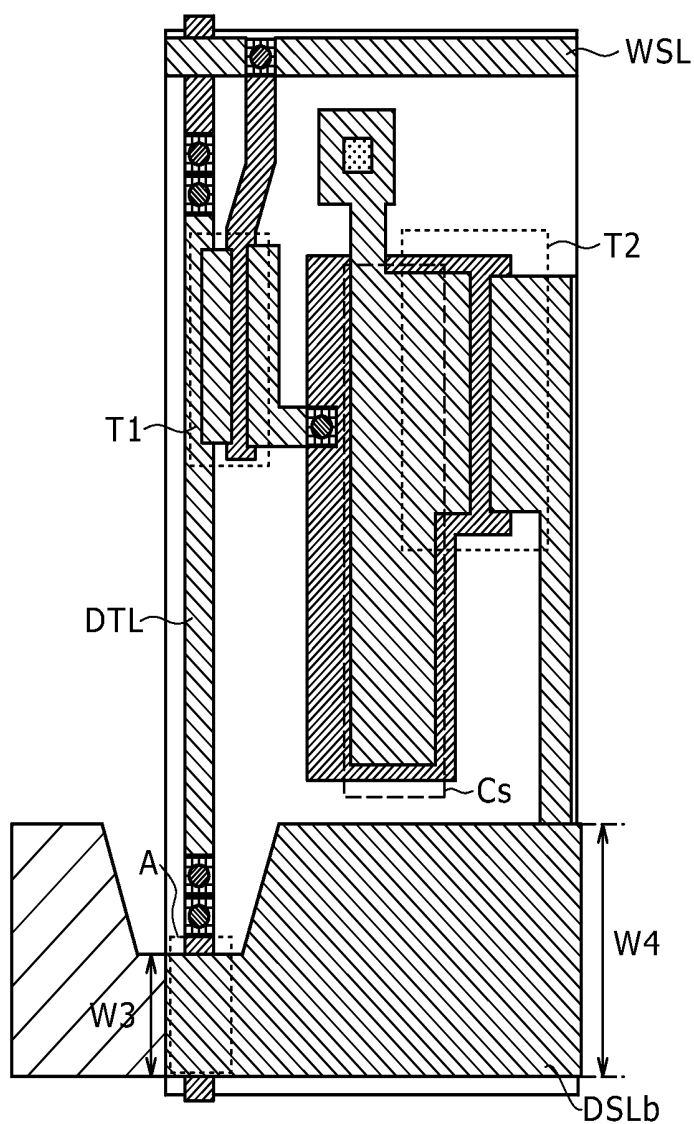


FIG. 27



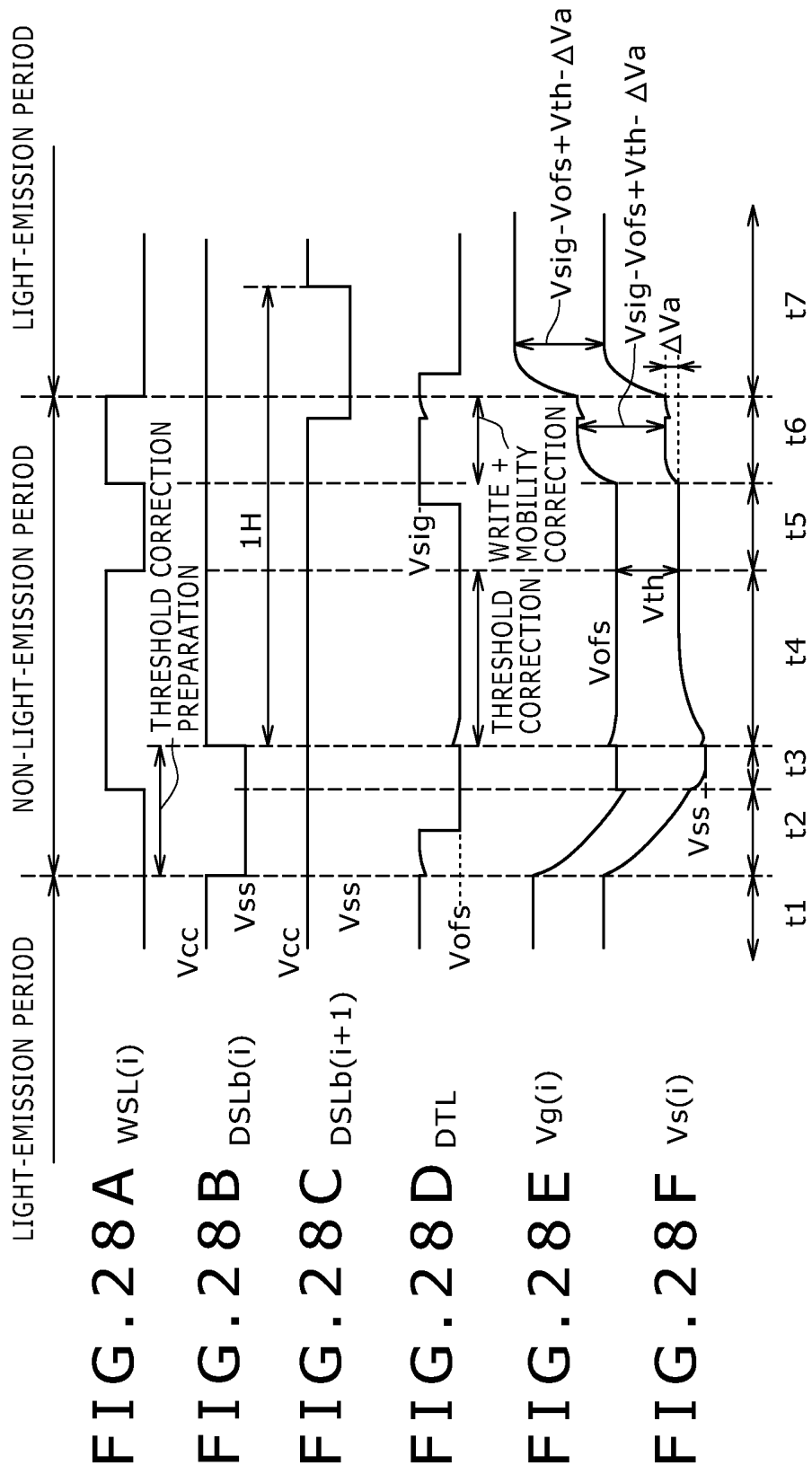
 FIRST METAL LAYER

 CONTACT BETWEEN FIRST METAL LAYER AND SECOND METAL LAYER

 SECOND METAL LAYER

 CONTACT BETWEEN SECOND METAL LAYER AND THIRD METAL LAYER

 FORMATION AREA OF HOLD CAPACITOR



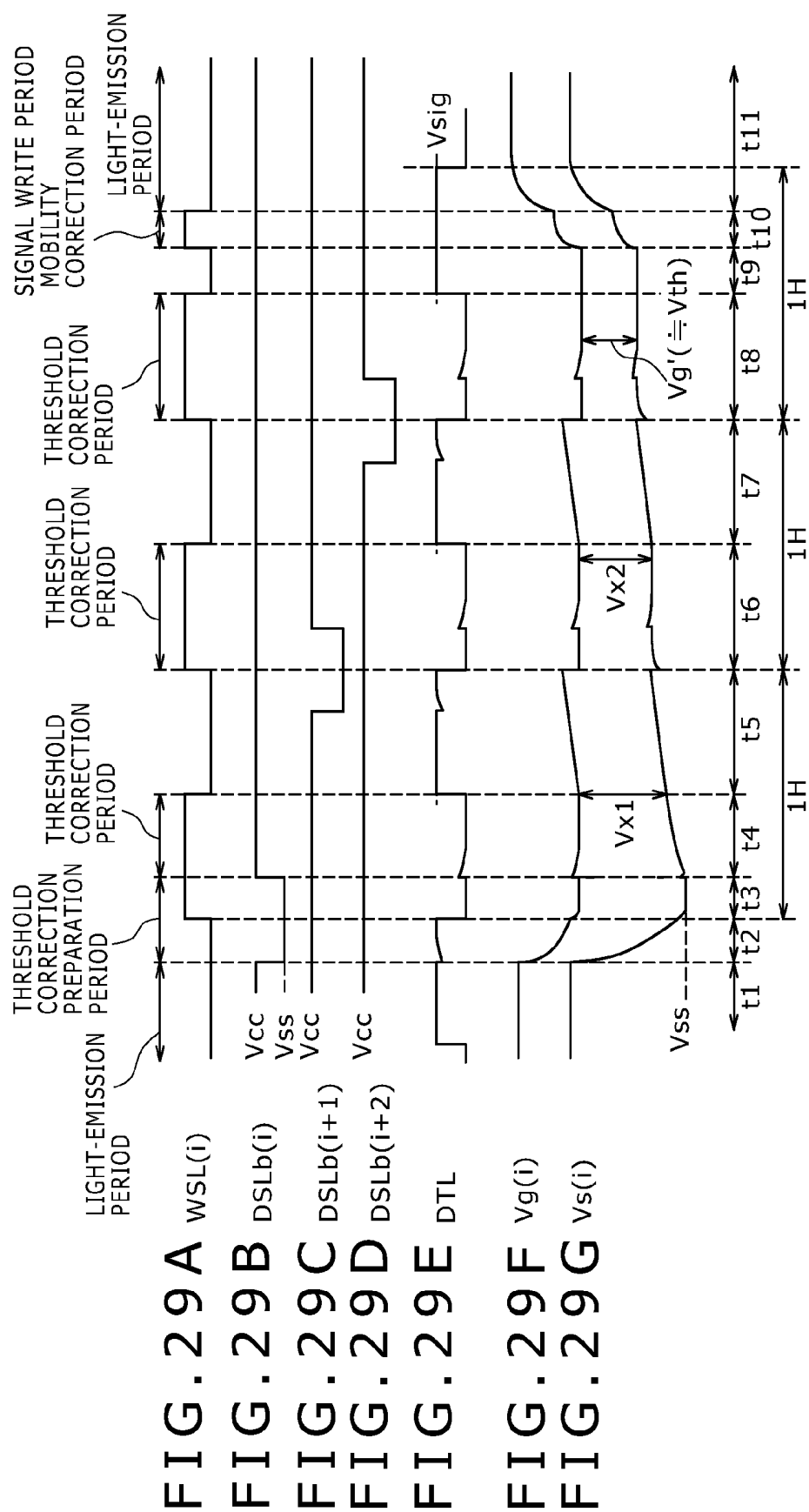
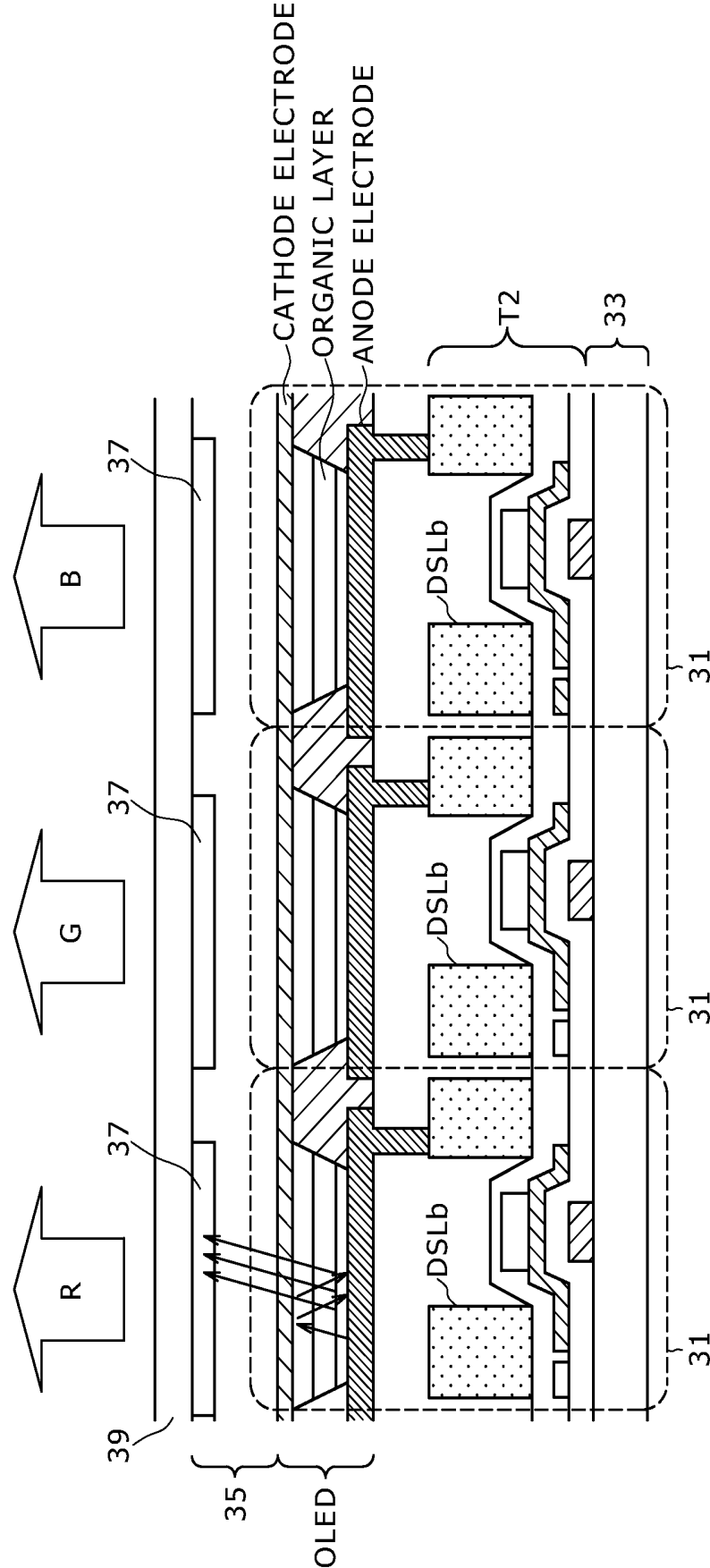


FIG. 30



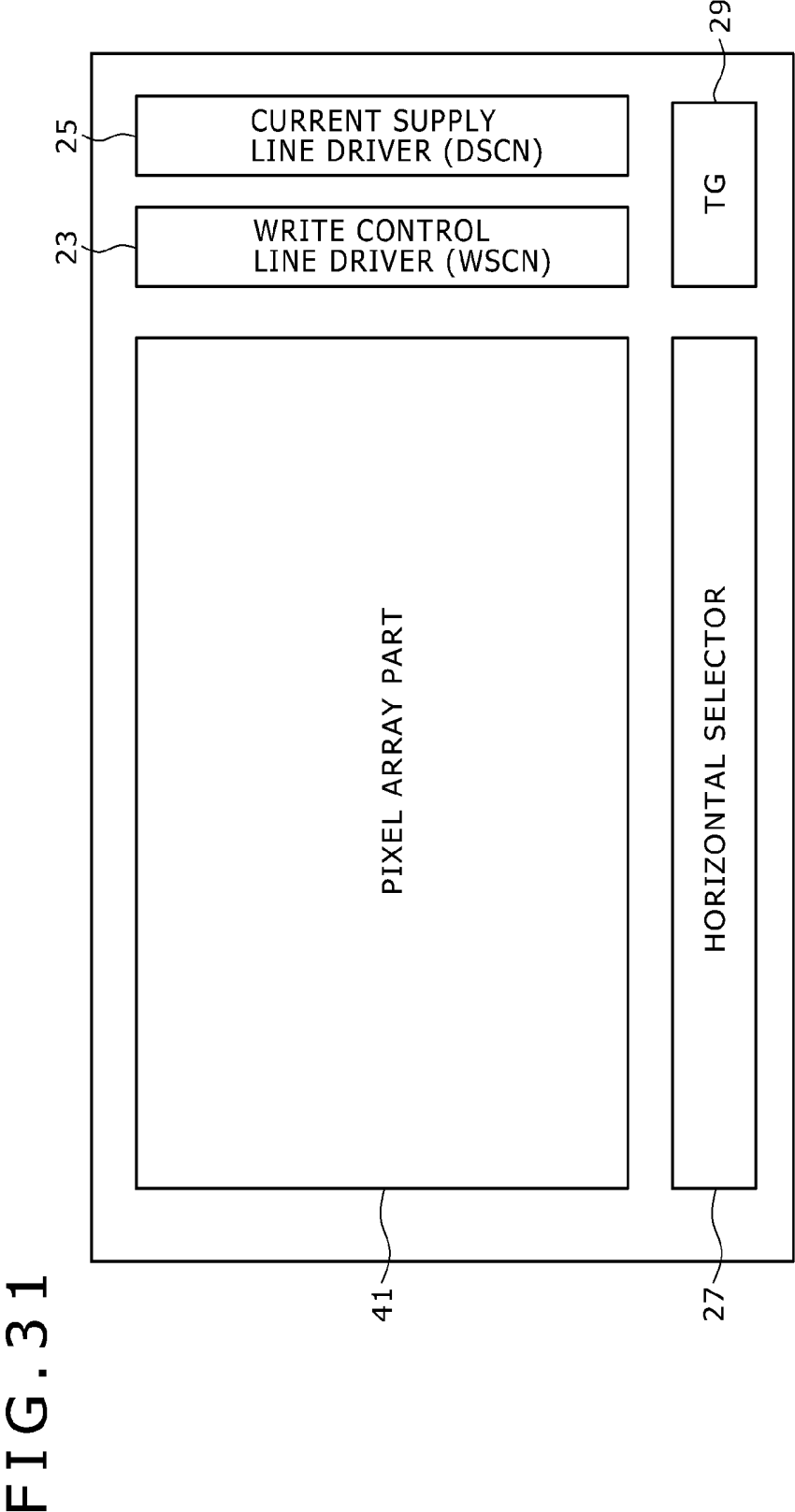


FIG. 33

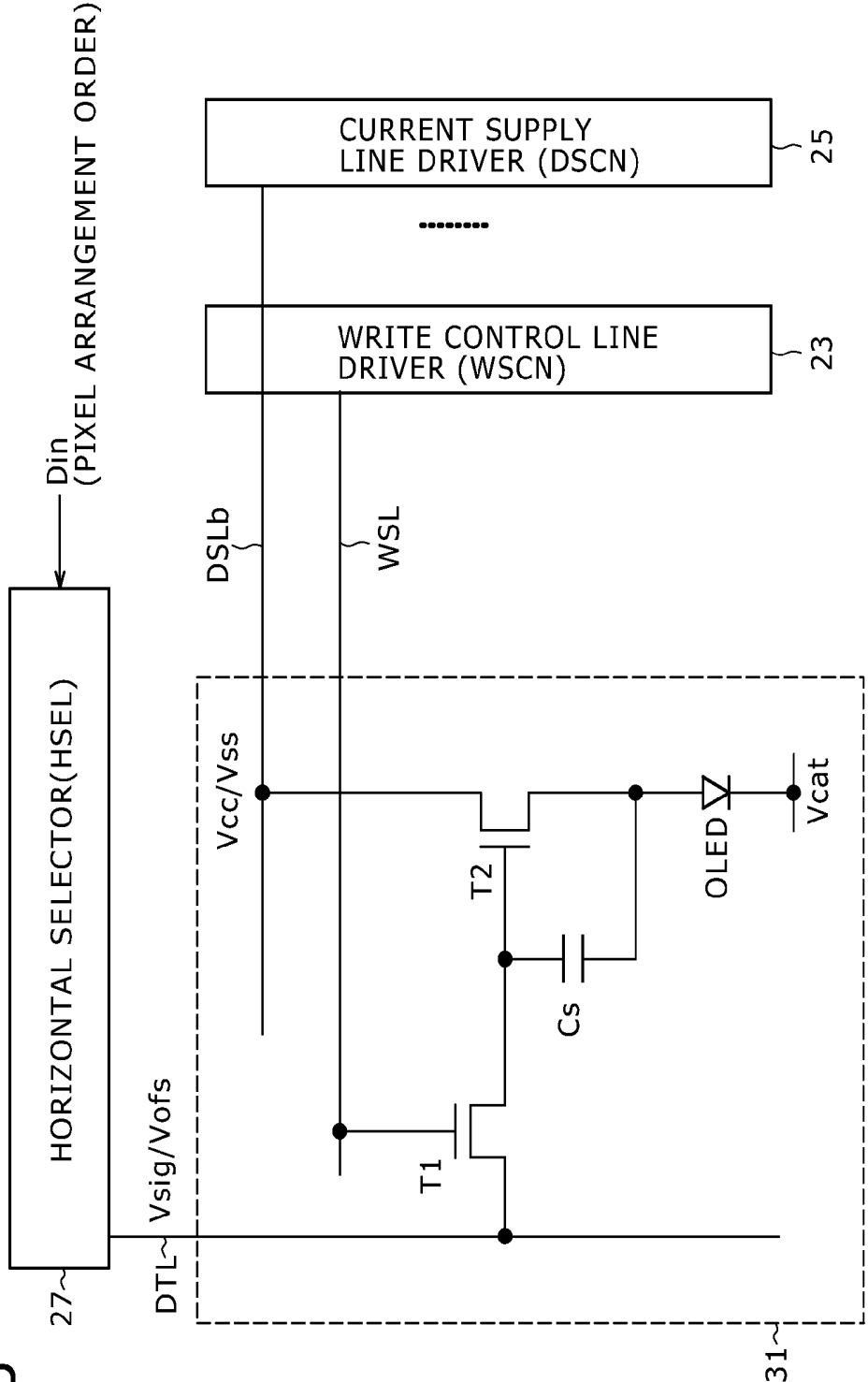


FIG. 34

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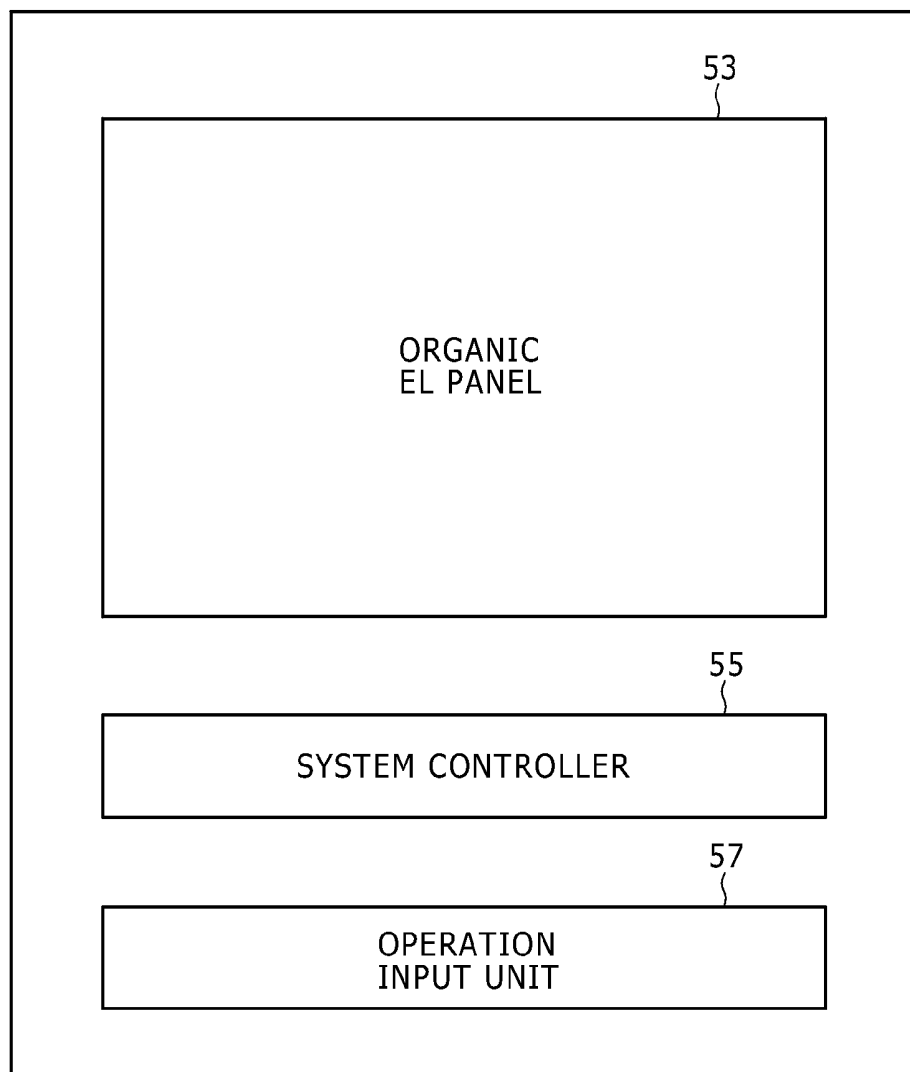
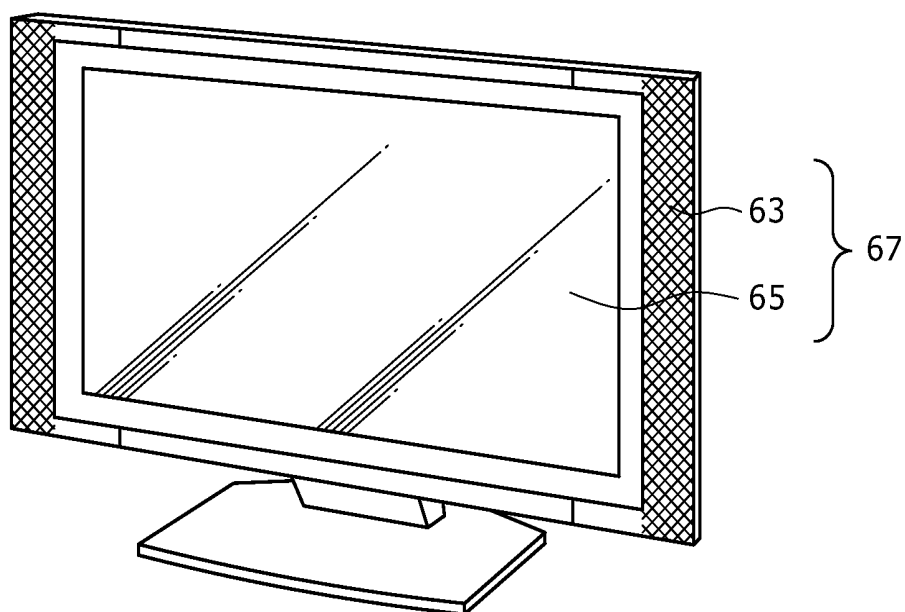


FIG. 35



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FIG. 36A

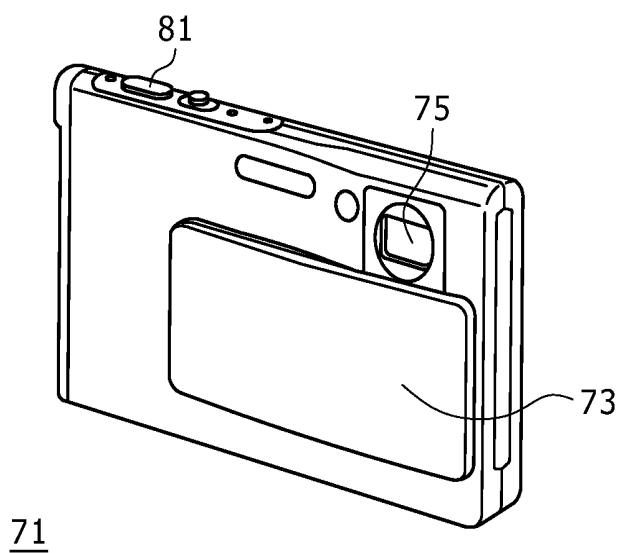


FIG. 36B

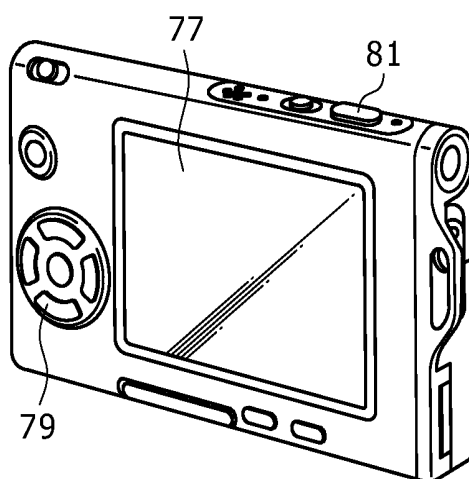
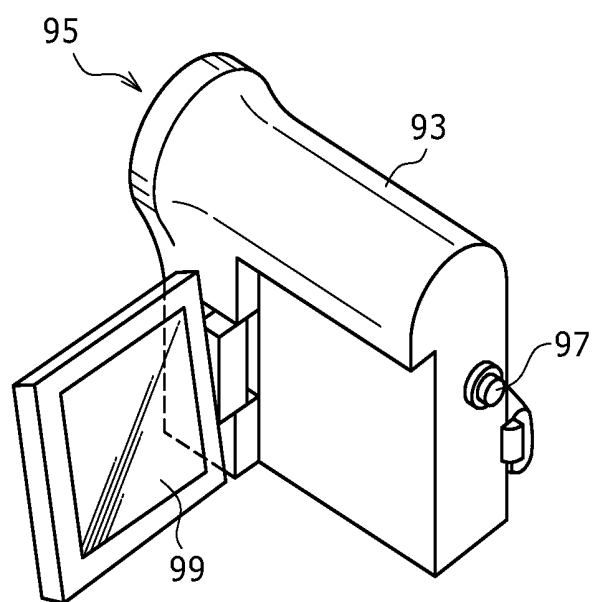


FIG. 37



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FIG. 38A

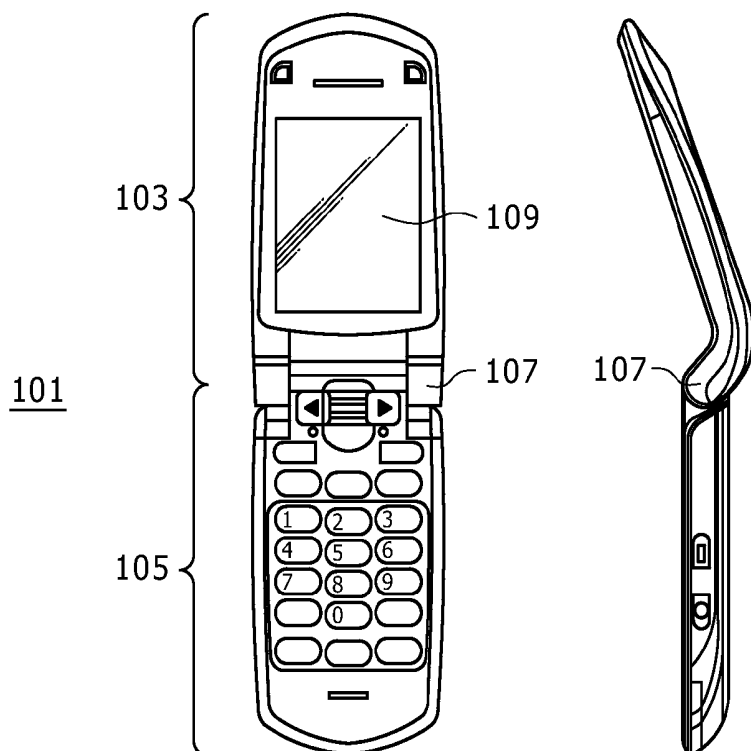


FIG. 38B

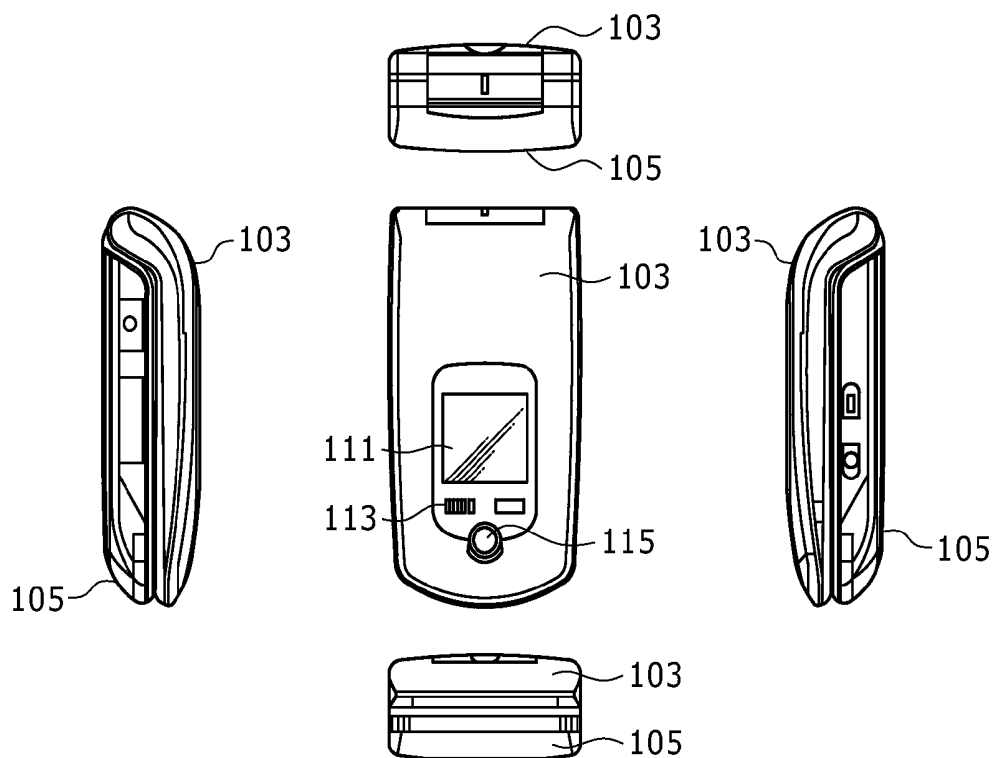
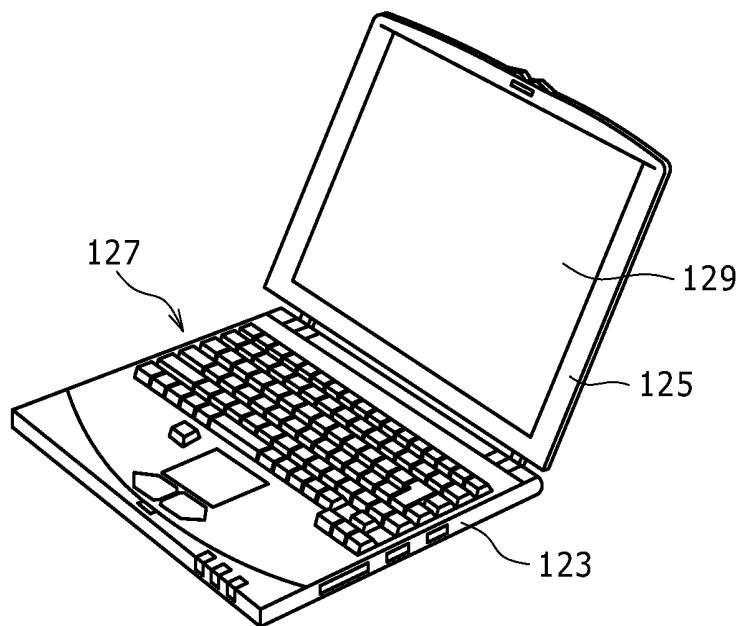


FIG. 39



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ELECTRO LUMINESCENT DISPLAY PANEL AND ELECTRONIC APPARATUS

CROSS REFERENCES TO RELATED APPLICATIONS

[0001] This is a Continuation application of U.S. patent application Ser. No. 12/292,339, filed Nov. 17, 2008, which in turn claims priority from Japanese Application No.: 2007-307042 filed in the Japan Patent Office on Nov. 28, 2007, the entire contents of which being incorporated herein by reference.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The invention to be described in this specification relates to the structure of an Electro luminescent (EL) display panel whose driving is controlled based on an active-matrix drive system. The invention to be proposed by this specification also has aspects as an EL display panel and electronic apparatus.

[0004] 2. Description of Related Art

[0005] FIG. 1 shows a general circuit block configuration of an active-matrix-driven organic EL panel. As shown in FIG. 1, an organic EL panel 1 includes a pixel array part 3, and a write control line driver 5 and a horizontal selector 7 as drive circuits for the pixel array part 3. In the pixel array part 3, pixel circuits 9 are disposed at the respective intersections of signal lines DTL and write control lines WSL.

[0006] An organic EL element is a current-driven light-emitting element. Therefore, in the organic EL panel, the grayscales of color representation are controlled through control of the amounts of the currents that flow through the organic EL elements corresponding to the respective pixels.

[0007] FIG. 2 shows one of the simplest circuit configurations of this kind of pixel circuit 9. This pixel circuit 9 includes a write transistor T1, a drive transistor T2, and a hold capacitor Cs.

[0008] The write transistor T1 is a thin film transistor that controls writing of a signal potential Vsig dependent upon the grayscale of the corresponding pixel to the hold capacitor Cs. The drive transistor T2 is a thin film transistor that supplies a drive current Ids to an organic EL element OLED based on a gate-source voltage Vgs dependent upon the signal potential Vsig held in the hold capacitor Cs. In the configuration of FIG. 2, the write transistor T1 is formed of an N-channel thin film transistor, and the drive transistor T2 is formed of a P-channel thin film transistor.

[0009] In the configuration of FIG. 2, the source electrode of the drive transistor T2 is connected to a current supply line (power supply line) to which a supply potential Vcc is fixedly applied. Therefore, the drive transistor T2 always operates in the saturation region. Specifically, the drive transistor T2 operates as a constant current source that supplies the drive current dependent upon the signal potential Vsig to the organic EL element OLED. The drive current Ids supplied by the drive transistor T2 is represented by the following equation.

$$I_{ds} = k \mu (V_{gs} - V_{th})^2 / 2$$

[0010] In this equation, μ denotes the mobility of the majority carrier in the drive transistor T2. V_{th} denotes the threshold voltage of the drive transistor T2. k is a coefficient represented

as $(W/L) \cdot Cox$. W denotes the channel width, L denotes the channel length, and Cox denotes the gate capacitance per unit area.

[0011] In the pixel circuit having this configuration, the drain voltage of the drive transistor T2 changes along with aging change in the I-V characteristic of the organic EL element, shown in FIG. 3.

[0012] However, because the gate-source voltage Vgs is kept constant, no change occurs in the amount of the current supplied to the organic EL element, and thus the light-emission luminance can be kept constant.

[0013] Examples of documents about an organic EL panel display employing the active-matrix drive system include Japanese Patent Laid-open Nos. 2003-255856, 2003-271095, 2004-133240, 2004-029791, and 2004-093682.

SUMMARY OF THE INVENTION

[0014] Depending on the kind of thin film process, the circuit configuration shown in FIG. 2 can not be employed in some cases. Specifically, the existing thin film processes involve the case in which a P-channel thin film transistor can not be employed. In such a case, the P-channel transistor as the drive transistor T2 is replaced by an N-channel thin film transistor.

[0015] FIG. 4 shows the configuration of this kind of pixel circuit. In this configuration, the source electrode of the drive transistor T2 is connected to the anode terminal of the organic EL element OLED. Therefore, this pixel circuit 9 involves a problem that the gate-source voltage Vgs of the drive transistor T2 varies in linkage with change in the I-V characteristic of the organic EL element along with time elapse. This change in the gate-source voltage Vgs leads to change in the drive current amount, resulting in change in the light-emission luminance.

[0016] In addition, the threshold voltage and the mobility of the drive transistor T2 included in each pixel circuit differ from pixel to pixel. The difference in the threshold voltage and the mobility of the drive transistor T2 appears as variation in the drive current value, which causes variation of the light-emission luminance of the pixels.

[0017] Therefore, if the pixel circuit shown in FIG. 4 is employed, establishment of a drive method that allows stable light-emission characteristics irrespective of aging change is required. At the same time, realization of a panel structure that offers high display quality is required.

[0018] The present inventors propose an EL display panel including a current supply line connected to a plurality of pixel circuits in common as an EL display panel having a pixel structure corresponding to an active-matrix drive system. In this EL display panel, the line width of an intersection part of the current supply line with a signal line is smaller than the line width of the other part of the current supply line.

[0019] According to this panel structure, without increasing the area of the intersection part of the current supply line with the signal line, the line width of the current supply line other than the intersection part can be increased. This means an advantage that the interconnect resistance of the current supply line as a whole can be decreased. As a result, potential change of the current supply line dependent upon a displayed image and pixel positions can be reduced.

[0020] Larger effects can be expected by this panel structure when driving of the current supply line is controlled with potentials of binary values or more values. In the case in which a fixed potential is not applied to the current supply

line, potential change of the current supply line is easily transmitted to the signal line via the coupling capacitance formed at the intersection part with the signal line if the area of the intersection part with the signal line is large.

[0021] However, according to the above-described panel structure, the area of the intersection part between the current supply line and the signal line can be decreased with respect to the current drive capability. Thus, the influence of potential change of the current supply line on the signal line can be decreased. As a result, the potential change transmitted to the signal line is small, and thus the influence on the potential that is being written can be minimized. Consequently, the lowering of the display quality can be suppressed.

[0022] The proposed panel structure is more effective when the pixel structure has a top-emission structure. In the top-emission structure, the forming layer of the current supply line does not intersect with the output paths of light rays. Therefore, the line width of the current supply line other than the intersection part with the signal line can be increased without influence on the aperture ratio.

[0023] Larger effects can be expected by the proposed panel structure when the timing of potential change of the current supply line corresponding to a certain row exists in a period of writing of a signal line potential on another row. As described above, the area of the intersection part with the signal line is small although potential change of the current supply line is transmitted via the intersection part with the signal line. Thus, the influence on the writing of the signal line potential in the pixel circuit on another row can be minimized.

[0024] In particular, if mobility correction is carried out in the period of the writing of the signal line potential, the accuracy of the mobility correction for the drive transistor can be enhanced. In addition, if threshold correction is carried out, the accuracy of the threshold correction for the drive transistor can be enhanced. Thus, the above-described panel structure is effective for suppressing the lowering of the display quality.

[0025] The present inventors also propose electronic apparatus including an EL display panel having the above-described panel structure.

[0026] The electronic apparatus includes the EL display panel, a system controller that controls the operation of the entire system, and an operation input unit that accepts an operation input to the system controller.

[0027] Employing the embodiments of the present invention proposed by the present inventors makes it possible to increase the line width of the current supply line other than the intersection part of the current supply line with the signal line without increasing the area of the intersection part. This increase in the line width allows reduction in the interconnect resistance of the current supply line as a whole. As a result, the image quality can be improved through suppression of the potential drop of the current supply line dependent upon a displayed image and pixel positions.

[0028] Furthermore, the area of the intersection part between the current supply line and the signal line can be decreased. This can suppress the amount of transmission of potential change from the current supply line to the signal line. Thus, erroneous writing to the pixel circuit due to change in the signal line potential can be prevented.

BRIEF DESCRIPTION OF THE DRAWINGS

[0029] FIG. 1 is a diagram for explaining the functional block configuration of an organic EL panel;

[0030] FIG. 2 is a diagram for explaining the connection relationship between a pixel circuit and drive circuits;

[0031] FIG. 3 is a diagram for explaining aging change in the I-V characteristic of an organic EL element;

[0032] FIG. 4 is a diagram showing another pixel circuit example;

[0033] FIG. 5 is a diagram showing an appearance configuration example of an organic EL panel;

[0034] FIG. 6 is a diagram showing a system configuration example of the organic EL panel;

[0035] FIG. 7 is a diagram for explaining the connection relationship between pixel circuits and drive circuits;

[0036] FIG. 8 is a diagram showing a configuration example of a pixel circuit according to a first form example;

[0037] FIGS. 9A to 9E are diagrams showing drive operation examples according to the first form example;

[0038] FIG. 10 is a diagram for explaining the operation state of the pixel circuit;

[0039] FIG. 11 is a diagram for explaining the operation state of the pixel circuit;

[0040] FIG. 12 is a diagram for explaining the operation state of the pixel circuit;

[0041] FIG. 13 is a diagram for explaining the operation state of the pixel circuit;

[0042] FIG. 14 is a diagram showing the rise of the source potential;

[0043] FIG. 15 is a diagram for explaining the operation state of the pixel circuit;

[0044] FIG. 16 is a diagram showing difference in the degree of the rise of the source potential due to difference in the mobility;

[0045] FIG. 17 is a diagram for explaining the operation state of the pixel circuit;

[0046] FIG. 18 is a diagram for explaining a shading phenomenon;

[0047] FIG. 19 is a diagram for explaining the cause of the occurrence of the shading phenomenon;

[0048] FIGS. 20A and 20B are diagrams for explaining a crosstalk phenomenon;

[0049] FIG. 21 is a diagram for explaining the cause of the occurrence of the crosstalk phenomenon;

[0050] FIG. 22 is a diagram showing the layout of the pixel circuit corresponding to the first form example;

[0051] FIG. 23 is a diagram showing an improved layout example of the pixel circuit;

[0052] FIGS. 24A to 24F are diagrams for explaining the influence of potential change of a current supply line on mobility correction;

[0053] FIGS. 25A to 25G are diagrams for explaining the influence of potential changes of current supply lines on threshold correction;

[0054] FIGS. 26A to 26D are diagrams for explaining the principle of the occurrence of the influence on the threshold correction;

[0055] FIG. 27 is a diagram showing the layout of a pixel circuit proposed as a second form example;

[0056] FIGS. 28A to 28F are diagrams for explaining improvement in the mobility correction;

[0057] FIGS. 29A to 29G are diagrams for explaining improvement in the threshold correction;

[0058] FIG. 30 is a diagram for explaining a top-emission structure example;

[0059] FIG. 31 is a diagram showing a configuration example of an organic EL panel according to the second form example;

[0060] FIG. 32 is a diagram showing the connection relationship between pixel circuits and drive circuits according to the second form example;

[0061] FIG. 33 is a diagram showing a configuration example of the pixel circuit according to the second form example;

[0062] FIG. 34 is a diagram showing a conceptual configuration example of electronic apparatus;

[0063] FIG. 35 is a diagram showing a commercial product example of electronic apparatus;

[0064] FIGS. 36A and 36B are diagrams showing commercial product examples of electronic apparatus;

[0065] FIG. 37 is a diagram showing a commercial product example of electronic apparatus;

[0066] FIGS. 38A and 38B are diagrams showing a commercial product examples of electronic apparatus; and

[0067] FIG. 39 is a diagram showing a commercial product example of electronic apparatus.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0068] The following description will deal with an example in which an embodiment of the present invention is applied to an active-matrix-driven organic EL panel.

[0069] Well-known or publicly-known techniques in the related-art technical field are applied to part that is not particularly illustrated or described in the present specification. It should be noted that the following form examples of the present invention are merely embodiment examples of the invention, and the invention is not limited thereto.

(A) Appearance Configuration

[0070] In this specification, not only a display panel obtained by forming a pixel array part and drive circuits on the same substrate by using the same semiconductor process but also e.g. one obtained by mounting drive circuits manufactured as application-specific ICs on a substrate on which a pixel array part is formed is referred to as an organic EL panel.

[0071] FIG. 5 shows an appearance configuration example of an organic EL panel. An organic EL panel 11 has a structure obtained by bonding a counter unit 15 to the formation area of a pixel array part of a support substrate 13.

[0072] The support substrate 13 is composed of glass, plastic, or another material, and an organic EL layer, a protective film, and so on are formed on the surface thereof. The base of the counter unit 15 is composed of glass, plastic, or another transparent material. In the organic EL panel 11, a flexible printed circuit (FPC) 17 for inputting/outputting of signals and so on from/to the external to/from the support substrate 13 is disposed.

(B) First Form Example

(B-1) System Configuration

[0073] The following description will deal with a system configuration example of the organic EL panel 11 in which variation in the characteristics of the drive transistor T2 formed of an N-channel thin film transistor is prevented and the number of elements included in the pixel circuit is small.

[0074] FIG. 6 shows the system configuration example of the organic EL panel 11. The organic EL panel 11 shown in FIG. 6 includes a pixel array part 21, and a write control line driver 23, a current supply line driver 25, a horizontal selector 27, and a timing generator 29 as drive circuits for the pixel array part 21.

[0075] The pixel array part 21 has a matrix structure in which sub-pixels are disposed at the respective intersections of signal lines DTL and write control lines WSL. The sub-pixel is the minimum unit of the pixel structure of one pixel. For example, one pixel as a white unit is composed of three sub-pixels (R, G, B) that are different from each other in the organic EL material.

[0076] FIG. 7 shows the connection relationship between the pixel circuits corresponding to the sub-pixels and the respective drive circuits. FIG. 8 shows the internal configuration of the pixel circuit to be proposed as a first form example. The pixel circuit shown in FIG. 8 includes two N-channel thin film transistors T1 and T2 and one hold capacitor Cs.

[0077] Also in this circuit configuration, the write control line driver 23 controls opening/closing of the write transistor T1 via the write control line WSL, to thereby control writing of a signal line potential to the hold capacitor Cs. The write control line driver 23 includes shift registers having the same number of output stages as the vertical solution.

[0078] The current supply line driver 25 controls, in a binary manner, a current supply line DSLa connected to one main electrode of the drive transistor T2, and controls the operation in the pixel circuit through cooperative operation together with other drive circuits. The operation in the pixel circuit encompasses not only the light-emission/non-light-emission operation of the organic EL element but also operation for correction against characteristic variations. In this form example, the correction against the characteristic variations means correction against the deterioration of the uniformity due to variations in the threshold voltage and the mobility of the drive transistor T2.

[0079] The horizontal selector 27 applies, to the signal line DTL, a signal potential Vsig dependent upon pixel data Din or an offset potential Vofs for threshold voltage correction. The horizontal selector 27 includes shift registers having the same number of output stages as the horizontal solution, latch circuits corresponding to the respective output stages, a D/A conversion circuit, a buffer circuit, and a selector.

[0080] The timing generator 29 produces the timing pulses necessary for the driving of the write control line WSL, the current supply line DSLa, and the signal line DTL.

(B-2) Drive Operation Example

[0081] FIGS. 9A to 9E show drive operation examples of the pixel circuit shown in FIG. 8. In FIGS. 9A to 9E, of two kinds of supply potentials applied to the current supply line DSLa, the higher potential (light-emission potential) is represented as Vcc, and the lower potential (non-light-emission potential) is represented as Vss.

[0082] FIG. 10 shows the operation state in the pixel circuit in the light-emission state. In this state, the write transistor T1 is in the off-state. On the other hand, the drive transistor T2 operates in the saturation region and supplies the current Ids dependent upon the gate-source voltage Vgs to the organic EL element OLED (FIGS. 9A to 9E (t1)).

[0083] Next, the operation state of the non-light-emission state will be described below. At the start of the non-light-

emission state, the potential of the current supply line DSLa is switched from the higher potential Vcc to the lower potential Vss (FIGS. 9A to 9E (t2)). At this time, the light emission of the organic EL element is stopped if the threshold voltage Vthel of the organic EL element satisfies the relationship $V_{ss}-V_{cath}(\text{cathode potential}) < V_{thel}$.

[0084] The source potential Vs of the drive transistor T2 becomes the same as the potential of the current supply line DSLa. That is, the anode electrode of the organic EL element is charged to the lower potential Vss. FIG. 11 shows the operation state in the pixel circuit in the period t2. As shown by the dashed line in FIG. 11, the charges held in the hold capacitor Cs are discharged to the current supply line DSLa at this time.

[0085] Thereafter, in response to the switch of the write control line WSL to the higher potential after the transition of the potential of the signal line DTL to the offset potential Vofs for threshold correction, the gate potential of the drive transistor T2 is changed to the offset potential Vofs via the turned-on write transistor T1 (FIGS. 9A to 9E (t3)).

[0086] FIG. 12 shows the operation state in the pixel circuit in the period t3. In the period t3, the gate-source voltage Vgs of the drive transistor T2 is expressed as $V_{ofs}-V_{ss}$. This voltage is set higher than the threshold voltage Vth of the drive transistor T2. This is because threshold correction operation can not be carried out unless the relationship $V_{ofs}-V_{ss} > V_{th}$ is satisfied.

[0087] Subsequently, the potential of the current supply line DSLa is switched to the higher potential Vcc again (FIGS. 9A to 9E (t4)). Due to the switch of the potential of the current supply line DSLa to the higher potential Vcc, the anode potential Vel of the organic EL element OLED becomes the source potential Vs of the drive transistor T2.

[0088] FIG. 13 shows the operation state in the pixel circuit in the period t4. In FIG. 13, the organic EL element OLED is represented by an equivalent circuit. Specifically, it is represented by a diode and a parasitic capacitor Cel. In the period t4, the drive current Ids flowing through the drive transistor T2 is used to charge the hold capacitor Cs and the parasitic capacitor Cel as long as the relationship $Vel < V_{cat}+V_{thel}$ is satisfied (based on the assumption that the leakage current of the organic EL element is considerably smaller than the drive current Ids flowing through the drive transistor T2).

[0089] As a result, as shown in FIG. 14, the anode potential Vel of the organic EL element OLED rises up along with time elapse. Specifically, the source potential Vs of the drive transistor T2 starts to rise up, with the gate potential Vg thereof fixed at the offset potential Vofs. This operation is the threshold correction operation.

[0090] In due course, the gate-source voltage Vgs of the drive transistor T2 converges on the threshold voltage Vth. At this time, the relationship $Vel=V_{ofs}-V_{th} \leq V_{cat}+V_{thel}$ is satisfied.

[0091] Upon the end of the threshold correction period, the write transistor T1 is turned off again (FIGS. 9A to 9E (t5)).

[0092] Due to this turning-off, the gate potential Vg of the drive transistor T2 enters the floating state. However, the drive transistor T2 is in the cut-off state because the gate-source voltage Vgs has converged on the threshold voltage Vth, and therefore the drive current Ids does not flow.

[0093] Thereafter, the write transistor T1 is controlled to the on-state again after the timing necessary for the transition of the potential of the signal line DTL to the signal potential Vsig (FIGS. 9A to 9E (t6)). FIG. 15 shows the operation state

in the pixel circuit in the period t6. The signal potential Vsig is the potential supplied depending on the grayscale of the corresponding pixel.

[0094] In the period t6, the gate potential Vg of the drive transistor T2 shifts to the signal potential Vsig. That is, the gate-source voltage Vgs becomes higher than the threshold voltage Vth. Thus, the drive transistor T2 enters the on-state, so that the drive current Ids starts to flow so as to charge the hold capacitor Cs and the parasitic capacitor Cel.

[0095] In response to the start of the supply of the drive current Ids, the source potential Vs of the drive transistor T2 rises up. The drive current Ids supplied by the drive transistor T2 is used to charge the hold capacitor Cs and the parasitic capacitor Cel as long as the source potential Vs of the drive transistor T2 is lower than the sum of the threshold voltage Vthel and the cathode voltage Vcat of the organic EL element (based on the assumption that the leakage current that flows into the organic EL element OLED is considerably smaller than the drive current Ids).

[0096] At the start timing of this operation, the threshold correction operation for the drive transistor T2 has been already completed. Therefore, the drive current Ids supplied from the drive transistor T2 has the value reflecting the mobility μ of the drive transistor T2. Specifically, when the drive transistor has higher mobility μ , the larger drive current Ids flows and the source potential Vs also rises up more rapidly.

[0097] In contrast, when the drive transistor has lower mobility μ , the smaller drive current Ids flows and the source potential Vs also rises up more slowly (FIG. 16).

[0098] As a result, the voltage held in the hold capacitor Cs is corrected depending on the mobility μ of the drive transistor T2. That is, the gate-source voltage Vgs of the drive transistor T2 is changed to the voltage resulting from the correction of the mobility μ .

[0099] At last, the write transistor T1 is turned off, so that the writing of the signal potential Vsig is ended. At this time, the gate-source voltage Vgs ($=V_{sig}-V_{ofs}+V_{th}-\Delta V$) of the drive transistor T2 is higher than the threshold voltage Vth. Therefore, the supply of a drive current Ids' is continued and the light emission of the organic EL element OLED starts.

[0100] Due to the flowing of the drive current Ids' to the organic EL element OLED, the source potential Vs of the drive transistor T2 rises up to a potential Vx. FIG. 17 shows the operation state in the pixel circuit in the light-emission period.

[0101] In the light-emission period, the gate potential Vg of the drive transistor T2 is in the floating state. Therefore, due to bootstrap operation by the hold capacitor Cs, the gate potential Vg of the drive transistor T2 rises up, with the gate-source voltage Vgs kept constant (FIGS. 9A to 9E (t7)).

[0102] Also in the drive circuit proposed as the present form example, the I-V characteristic of the organic EL element OLED changes as the total light-emission time becomes longer. That is, the source potential Vs of the drive transistor T2 also changes.

[0103] However, no change occurs in the amount of the current that flows through the organic EL element OLED because the gate-source voltage Vgs of the drive transistor T2 is kept constant due to the hold capacitor Cs.

[0104] If the pixel circuit and the drive system proposed as the present form example are employed, it is possible to always supply the drive current Ids dependent upon the signal potential Vsig irrespective of change in the I-V characteristic of the organic EL element OLED.

[0105] That is, the light-emission luminance can be continuously kept at the luminance dependent upon the signal potential V_{sig} irrespective of aging change in the characteristics of the organic EL element OLED.

(B-3) Summary

[0106] As above, by employing the pixel circuit and the drive system described for the present form example, an organic EL panel free from variation in the luminance from pixel to pixel can be achieved even when the drive transistor T2 is formed of an N-channel thin film transistor. Furthermore, the pixel circuit can be formed by using only N-channel thin film transistors, which makes it possible to employ an amorphous silicon process for the manufacturing of the organic EL panel.

(C) Second Form Example

(C-1) Discussion of Other Technical Problems

[0107] As described above, the organic EL element OLED is a current-driven element. Therefore, the drive current I_{ds} necessary for the respective pixel circuits cumulatively flows through the current supply line DSLa. FIG. 18 shows the relationship between pixel positions and voltage drops when the current supply line DSLa extends in parallel to the horizontal lines. In FIG. 18, the resistive component of the current supply line DSLa is expressly shown.

[0108] Due to the influence of the resistive component shown in FIG. 18, the amount of the voltage drop in the current supply line DSLa becomes larger gradually as the pixel position becomes farther from the current supply line driver 25. This is because the voltage drop per one pixel is represented as the product of the drive current I_{ds} corresponding to the pixel circuit and the interconnect resistance per one pixel. Naturally, a supply potential V_y of the pixel circuit at the right end of the screen is lower than a supply potential V_x of the pixel circuit at the left end of the screen.

[0109] This supply potential lowering acts to decrease the drain-source voltage V_{ds} of the drive transistor T2 included in the pixel circuit.

[0110] FIG. 19 shows the influence on the drive current I_{ds} due to the difference in the supply potential between the right end and the left end of the screen. As shown in FIG. 19, even if the grayscale is the same, difference in the light-emission luminance arises if the drive current I_{ds} is different. This phenomenon is perceived as the shading phenomenon.

[0111] This phenomenon called shading is attributed to the interconnect structure of the current supply line DSLa as described above. Therefore, it is impossible for the functions to correct the characteristics of the drive transistor T2, described for the first form example, to prevent the occurrence of the shading phenomenon.

[0112] In addition, the shading phenomenon also relates to the occurrence of crosstalk.

[0113] The crosstalk refers to a phenomenon in which, when an image like that shown in FIG. 20A (such as an image in which a black-displayed window is disposed in a partial area of an all-white-background image) is displayed, luminance difference among the horizontal lines is perceived as shown in FIG. 20B. Specifically, the luminance difference arises between the background-white part on the same horizontal line as that of the black-displayed window and the

background-white parts on the horizontal lines on the upper and lower sides of the black-displayed window.

[0114] This luminance difference is attributed to the state in which no drive current I_{ds} flows in the pixel circuits corresponding to the black-displayed window part as shown in FIG. 21. Specifically, this luminance difference is attributed to the state in which the voltage drop in the current supply line DSL in the black-displayed window part is very small. As a result, the voltage drop in the current supply line DSL near the screen right end on the same row as that of the black-displayed window part is very small, and thus high light-emission luminance is obtained.

[0115] On the other hand, near the screen right end on a horizontal line different from that of the black-displayed window, the voltage drop amount is large due to the accumulation of the voltage drops as shown in FIG. 21. That is, the light-emission luminance is lowered corresponding to the drop of the supply potential. As a result, even on the same right-end column, luminance difference arises between the horizontal line of the black-displayed window and other horizontal lines, and luminance difference larger than a certain amount is visually recognized.

[0116] The voltage drop amount is obtained as the sum of the products of the drive current and the interconnect resistance of the current supply line.

[0117] For example, in the case of the panel structure of FIG. 21, when the number of pixels (including all of R pixels, G pixels, and B pixels) on the horizontal line is defined as N, the maximum value of the drive current I_{ds} necessary for the respective pixels is defined as I, and the interconnect resistance per one pixel is defined as r, a voltage drop amount V_y of the current supply line DSL at the remotest position from the current supply line driver 25 (in the present form example, at the screen right end) is represented by the following equation.

$$V_y = \{N(N+1)/2\} \cdot I \cdot r \quad (\text{Equation 1})$$

[0118] Therefore, the voltage drop amount can be decreased if at least one of N, I, and r is decreased.

[0119] In the following, a discussion will be made on the scheme of decreasing the interconnect resistance r. To decrease the interconnect resistance r, it is necessary to increase the interconnect width of the current supply line DSL or increase the thickness of the metal film (e.g. aluminum film) of the current supply line DSL.

[0120] Of these methods, the method of increasing the thickness involves change of the process, which possibly causes the lowering of the production takt and the yield, and so on. Therefore, the other method should be selected. Specifically, the method of increasing the line width of the current supply line DSL should be selected.

[0121] FIG. 22 shows a layout example of the pixel circuit 31 corresponding to the first form example. The same symbol in FIG. 22 as that in FIG. 8 indicates the same component. In FIG. 22, the line width of the current supply line DSLa is represented as W1.

[0122] FIG. 23 shows a layout example in which the line width of the current supply line DSLa is increased to W2 (>W1). If the layout of FIG. 23 is employed, the interconnect resistance of the current supply line DSLa can be decreased. As a result, suppression of shading and crosstalk can be expected.

[0123] However, due to the increase in the line width of the current supply line DSLa, the area of the intersection part

between the current supply line DSLa and the signal line DTL (the part surrounded by the dashed line and given symbol A in FIG. 23) is increased.

[0124] This area increase leads to increase in the inter-line capacitance (coupling capacitance) formed between the current supply line DSLa and the signal line DTL. That is, the area increase causes another technical problem that potential change of the current supply line DSLa is easily transmitted to the signal line DTL.

[0125] For example, at the timing of writing of the signal potential Vsig in the pixel circuit corresponding to a certain horizontal line, the potential of the current supply line DSLa corresponding to another horizontal line possibly changes. In this case, the mobility correction for the drive transistor T2 will be incorrectly carried out unless the potential changes of the gate and the source of the drive transistor T2 due to the potential change of the current supply line DSLa are cancelled within the mobility correction period.

[0126] FIGS. 24A to 24F show drive operation examples of the pixel circuit 31 corresponding to a certain horizontal line. The position of the horizontal line of interest is represented by a suffix "i." The suffix "i" indicates the horizontal line on the i-th row from the uppermost row on the screen.

[0127] FIG. 24A shows a signal waveform example of the write control line WSL(i) of the pixel circuit 31 corresponding to the i-th horizontal line. FIG. 24B shows a signal waveform example of the current supply line DSLa(i) corresponding to the i-th horizontal line. FIG. 24C shows a signal waveform example of the current supply line DSLa(i+1) corresponding to the i+1-th horizontal line.

[0128] FIG. 24D shows the signal waveform of the signal line DTL that intersects with the current supply lines. FIG. 24E shows the signal waveform of the gate potential Vg of the drive transistor T2 included in the pixel circuit 31 corresponding to the i-th horizontal line. FIG. 24F shows the signal waveform of the source potential Vs of the drive transistor T2 included in the pixel circuit 31 corresponding to the i-th horizontal line.

[0129] As shown in FIG. 24D, potential change of the current supply line DSLa is transmitted to the signal line DTL(i) via the interconnect capacitance of the intersection part irrespective whether this potential change occurred on the same row as that of the pixel circuit as the mobility correction target or occurred on another row. From FIGS. 24A to 24F, a phenomenon can be found in which change in the supply potential (change from the higher potential Vcc to the lower potential Vss) in the period of writing of the signal potential Vsig and mobility correction (t6) affects the gate potential Vg and the source potential Vs of the drive transistor T2.

[0130] Nevertheless, if the gate potential Vg and the source potential Vs return to the original potentials in the mobility correction period, the mobility correction operation can be completed without any problem. However, unless these potentials return to the original potentials, the mobility correction operation can not be correctly completed.

[0131] This is because the potential change amount of the source potential Vs is smaller than that of the gate potential Vg due to the intermediary of the hold capacitor Cs.

[0132] Specifically, unless the change in the gate potential Vg is cancelled in the mobility correction period, the gate-source voltage Vgs of the drive transistor T2 becomes lower than that obtained through normal mobility correction. This means that the screen luminance becomes lower than the original luminance level.

[0133] In addition, the amount of the potential change due to the influence of the coupling is constant irrespective of the signal potential Vsig.

[0134] Therefore, when the signal potential Vsig has a value for low luminance, the lowering of the luminance level has serious influence. This causes image quality lowering as erroneous expression of lower-side grayscales as 100% black and insufficiency in gamma correction.

[0135] In addition, the transmission of potential change to the signal line DTL often affects the pixel circuit driving when the threshold correction period is divided into plural periods in plural horizontal scanning periods.

[0136] For example, in the threshold correction period for the pixel circuit corresponding to a certain horizontal line, the potential of the current supply line DSLa corresponding to another horizontal line possibly changes. In this case, the threshold correction for the drive transistor T2 will be incorrectly carried out unless the potential changes of the gate and the source of the drive transistor T2 due to the potential change of the current supply line DSLa are cancelled within the threshold correction period.

[0137] FIGS. 25A to 25G show drive operation examples of the pixel circuit 31 corresponding to a certain horizontal line. Specifically, FIGS. 25A to 25G show an operation example in which threshold correction operation is executed in three horizontal scanning periods in a divided manner. Also in FIGS. 25A to 25G, the position of the horizontal line of interest is represented by a suffix "i." The suffix "i" indicates the horizontal line on the i-th row from the uppermost row on the screen.

[0138] FIG. 25A shows a signal waveform example of the write control line WSL(i) of the pixel circuit 31 corresponding to the i-th horizontal line. FIG. 25B shows a signal waveform example of the current supply line DSLa(i) corresponding to the i-th horizontal line. FIG. 25C shows a signal waveform example of the current supply line DSLa(i+1) corresponding to the i+1-th horizontal line.

[0139] FIG. 25D shows a signal waveform example of the current supply line DSLa(i+2) corresponding to the i+2-th horizontal line.

[0140] FIG. 25E shows the signal waveform of the signal line DTL that intersects with the current supply lines. FIG. 25F shows the signal waveform of the gate potential Vg of the drive transistor T2 included in the pixel circuit 31 corresponding to the i-th horizontal line. FIG. 25G shows the signal waveform of the source potential Vs of the drive transistor T2 included in the pixel circuit 31 corresponding to the i-th horizontal line.

[0141] As shown in FIG. 25E, potential change of the current supply line DSLa is transmitted to the signal line DTL via the interconnect capacitance of the intersection part irrespective whether this potential change occurred on the same row as that of the pixel circuit as the threshold correction target or occurred on another row. In the case of FIGS. 25A to 25G, changes in the supply potential (changes from the lower potential Vss to the higher potential Vcc) in the periods t3, t4, t6, and t8, during which the write transistor T1 is in the on-state, are transmitted to the gate potential Vg and the source potential Vs of the drive transistor T2.

[0142] Also in this case, if the potential changes of the gate potential Vg and the source potential Vs are cancelled in the threshold correction period, the threshold correction can be completed without any problem. However, if potential change of the current supply line DSLa on a different row is

transmitted immediately before the end of the threshold correction operation and thus the gate potential V_g and the source potential V_s are changed but not returned to the original potentials, the threshold correction operation can also not be correctly completed.

[0143] The reason for this is shown in FIGS. 26A to 26D. FIG. 26A shows the potential relationship in the pixel circuit before the occurrence of potential change of the current supply line DSLa. In the case of FIG. 26A, the gate-source voltage V_{gs} of the drive transistor T2 has already converged on the threshold voltage V_{th} . FIG. 26B shows the state after the potential of the current supply line DSLa is changed immediately before the end of the threshold correction period.

[0144] The gate potential V_g at this time is higher than the offset potential V_{ofs} by ΔV corresponding to the potential change. On the other hand, the change amount ΔV_s of the source potential V_s is smaller than the change amount ΔV of the gate potential V_g because the potential change is transmitted to the source via the hold capacitor C_s . Consequently, the gate-source voltage V_{gs} of the drive transistor T2 becomes higher than the threshold voltage V_{th} , and thus the drive transistor T2 is turned on again.

[0145] As a result, as shown in FIG. 26C, the mobility correction operation for the drive transistor T2 continues, so that the source potential V_s further rises up by $\Delta V_s'$.

[0146] In due course, as shown in FIG. 26D, when the influence of the potential change of the current supply line DSLa disappears, the gate potential V_g of the drive transistor T2 converges on the offset potential V_{ofs} and the source potential V_s converges on the potential higher by $\Delta V_s'$ than the potential before the potential change.

[0147] This means that the gate-source voltage V_{gs} of the drive transistor T2 has been changed to a voltage V_{gs}' lower than the threshold voltage V_{th} at the end timing of the threshold correction period.

[0148] That is, the threshold correction operation is not normally carried out. As a result, the light-emission luminance does not correspond with the original luminance.

[0149] In addition, the increase in the intersection area between the current supply line DSLa and the signal line DTL means increase in the overlapping area between the metal layers. Therefore, the increase in the intersection area also causes increase in the possibility of short-circuit of the layers.

[0150] Furthermore, as shown in FIG. 23, if the current supply line DSLa is formed as a layer (second layer) above the signal line DTL, the interconnect length of the layer part of the signal line DTL (first layer) under the current supply line DSLa is large. In this case, if the interconnect resistance of the under layer (first layer) part is higher than that of the upper layer (second layer), the interconnect resistance of the signal line DTL as a whole is high.

(C-2) Layout by Proposal

[0151] To address these problems, the present inventors propose a layout shown in FIG. 27. Specifically, in the interconnect structure of this layout, only the intersection part of a current supply line DSLb with the signal line DTL has a small line width $W3$ ($<W1$), whereas the other part of the current supply line DSLb has a large line width $W4$ ($>W1$).

[0152] Therefore, the small-width part and the large-width part of the current supply line DSLb alternately exist along the horizontal line with a cycle of the pixel pitch.

[0153] In the case of FIG. 27, the line width of the current supply line DSLb is gradually increased from the line width $W3$ to the line width $W4$ along the horizontal direction, and is gradually decreased from the line width $W4$ to the line width $W3$ along the horizontal direction.

[0154] Alternatively, the line width of the current supply line DSLb may be changed in a stepwise manner (with right-angle corners) between the line widths $W3$ and $W4$.

[0155] Using this interconnect structure can decrease the interconnect resistance of the current supply line DSLb as a whole and thus can effectively suppress the occurrence of shading and crosstalk.

[0156] The line widths $W3$ and $W4$ (particularly, $W4$) are so designed that the voltage drop amount V_y represented by Equation 1 is smaller than the limit value relating to visual recognition of crosstalk. The limit value relating to visual recognition of crosstalk differs depending on the use environment, the horizontal scanning cycle, and so on. As a measure of the limit value, e.g. 1% of the luminance corresponding to the highest grayscale is available.

[0157] Furthermore, the interconnect structure shown in FIG. 27 can solve the above-described other problems.

[0158] First, in the interconnect structure shown in FIG. 27, the inter-line capacitance formed between the current supply line DSLb and the signal line DTL is low. This is because the line width of the intersection part is decreased to $W3$. Therefore, transmission of potential change of the current supply line DSLb to the signal line DTL can be reduced.

[0159] Consequently, even if the potential of the current supply line DSLb corresponding to another horizontal line changes at the timing of writing of the signal potential V_{sig} in the pixel circuit corresponding to a certain horizontal line and thus potential change occurs in the signal potential V_{sig} that is being written, the potential change can be cancelled in the mobility correction period because the change itself is small. That is, normal mobility correction can be ensured.

[0160] FIGS. 28A to 28F show a drive operation example of the pixel circuit 31 corresponding to a certain horizontal line. FIGS. 28A to 28F are diagram corresponding to FIGS. 24A to 24F, and the position of the horizontal line of interest is represented by a suffix "i." Therefore, the signal waveforms of FIGS. 28A to 28F correspond to the signal waveforms of FIGS. 24A to 24F, respectively.

[0161] Naturally, also in the interconnect structure proposed by the present inventors, potential change of the current supply line DSLb is transmitted to the signal line DTL via the inter-line capacitance formed at the intersection part with the signal line DTL as shown in FIG. 28D. However, the transmission amount is smaller than that in FIGS. 24A to 24F.

[0162] Therefore, although the supply potential is changed from the higher potential V_{cc} to the lower potential V_{ss} in the period of the writing of the signal potential V_{sig} and the mobility correction ($t6$), the amounts of changes occurring in the gate potential V_g and the source potential V_s of the drive transistor T2 are small.

[0163] Thus, the gate potential V_g and the source potential V_s can be returned to the original potentials in the mobility correction period surely, and hence the mobility correction operation can be completed within the period. Therefore, not only when the signal potential V_{sig} has a value for high luminance but also when it has a value for low luminance, the original light-emission luminance corresponding to the grayscale can be achieved.

[0164] In addition, the suppression of the amount of potential change transmitted to the signal line DTL offers advantageous effects also when the threshold correction period is divided into plural periods in plural horizontal scanning periods.

[0165] This feature will be described below with reference to FIGS. 29A to 29G. FIGS. 29A to 29G are diagram corresponding to FIGS. 25A to 25G, and the position of the horizontal line of interest is represented by a suffix "i." Therefore, the signal waveforms of FIGS. 29A to 29G correspond to the signal waveforms of FIGS. 25A to 25G, respectively.

[0166] Also in the case of FIGS. 29A to 29G, potential changes of the current supply line DSLb (changes from the lower potential Vss to the higher potential Vcc) in the periods t3, t4, t6, and t8, during which the write transistor T1 is in the on-state, are transmitted to the gate potential Vg and the source potential Vs of the drive transistor T2.

[0167] However, the amounts of the transmission of the potential changes are very small because the inter-line capacitance (coupling capacitance) formed at the intersection part between the current supply line DSLb and the signal line DTL based on the interconnect structure proposed by the present inventors is low.

[0168] As a result, even if potential changes of the gate potential Vg and the source potential Vs occur immediately before the end of the threshold correction period, the changes can be cancelled in the remaining correction period, so that the threshold correction can be completed without any problem. Furthermore, even if potential change is transmitted after the completion of the threshold correction operation and the threshold correction operation is restarted, the amount ΔV_s of increase in the source potential Vs occurring at this time is so small as to be ignorable. Therefore, there is no need to consider the influence on the threshold correction operation.

[0169] In addition, in the interconnect structure shown in FIG. 27, the intersection area of the current supply line DSLb and the signal line DTL is small and thus the overlapping area of the metal layers is also small.

[0170] Therefore, an effect of decreasing the possibility of short-circuit of the layers can also be expected.

[0171] Furthermore, as shown in FIG. 27, if the current supply line DSLb is formed as a layer (second layer) above the signal line DTL, the interconnect length of the layer part of the signal line DTL (first layer) under the current supply line DSLb can be decreased.

[0172] Therefore, even if the interconnect resistance of the under layer (first layer) part is higher than that of the upper layer (second layer), the interconnect resistance of the signal line DTL as a whole can be decreased.

[0173] The above-described various advantageous effects are particularly large when the organic EL panel has a top-emission pixel structure.

[0174] FIG. 30 shows a sectional structural example of an organic EL panel having a top-emission structure. In this structure, the respective elements such as the write transistor T1, the drive transistor T2, and the hold capacitor Cs are formed over a glass substrate 33 as a support substrate, and the organic EL elements OLED are formed over these elements.

[0175] Over the organic EL elements OLED, a sealing material 35, color filters 37, and a glass substrate 39 are sequentially disposed.

[0176] In this layer structure, light output from an organic layer sequentially passes through the cathode electrode

formed of a semi-transparent film and the color filter 37 so as to be output to the external from the surface of the glass substrate 39, which seals these components.

[0177] In the top-emission structure, interconnect layers such as the current supply line DSLb and the signal line DTL are not disposed on the optical path. Specifically, the current supply line DSLb is disposed at a layer level lower than that of the organic EL elements OLED.

[0178] Therefore, in terms of ensuring of a high aperture ratio, there is no limit to the increase of the line width W4 of the current supply line DSLb at the part other than the intersection part with the signal line DTL, and thus the line width W4 can be increased to the necessary width.

(C-3) System Configuration

[0179] FIG. 31 shows a system configuration example of an organic EL panel 11 having the above-described interconnect structure. The same unit in FIG. 31 as that in FIG. 6 is given the same numeral.

[0180] The organic EL panel 11 shown in FIG. 31 includes a pixel array part 41, and the write control line driver 23, the current supply line driver 25, the horizontal selector 27, and the timing generator 29 as drive circuits for the pixel array part 41.

[0181] Of these units, the pixel array part 41 has the same structure as that of the pixel array part 21 described for the first form example except for the current supply line DSLb (FIG. 27). Specifically, the pixel array part 41 has a pixel structure in compatible with an active-matrix drive system for controlling the operation state of the pixel circuit based on driving of the current supply line DSLb with potentials of binary values.

[0182] Therefore, the connection relationship between the pixel circuits 31 and the respective drive circuits (FIG. 32) and the internal configuration of the pixel circuit 31 (FIG. 33) are the same as those in the first form example.

(D) Other Form Examples

(D-1) Drive System 1

[0183] In the above-described form examples, driving of the current supply line DSLb is controlled with potentials of binary values (the higher potential Vcc and the lower potential Vss).

[0184] However, it is obvious that the above-described interconnect structure can also be applied to a configuration in which driving of the current supply line DSLb is controlled with potentials of ternary values or more values. If the current supply line DSLb based on the above-described interconnect structure is used, transmission of potential change to the signal line DTL can be effectively suppressed also when driving of the current supply line DSLb is controlled with potentials of ternary values or more values.

(D-2) Drive System 2

[0185] In the above-described form examples, driving of the current supply line DSLb is controlled with potentials of binary values (the higher potential Vcc and the lower potential Vss).

[0186] However, the current supply line DSLb can also be employed for e.g. the pixel structures shown in FIGS. 2 and 4. Specifically, the above-described interconnect structure can

also be applied to a structure in which the current supply line DSLb is controlled to a fixed potential.

[0187] Also in this case, the interconnect resistance of the current supply line DSLb can be decreased, and thus the influence of shading and crosstalk can be reduced.

[0188] Furthermore, the area of the intersection part with the signal line DTL can be decreased, which can reduce the inter-line capacitance (coupling capacitance), the resistance of the signal line DTL, and so on.

(D-3) Drive System 3

[0189] In the above-described form examples, the timing of potential change of the current supply line DSLb corresponding to another horizontal line overlaps with the period of writing of the signal line potential (the signal potential Vsig or the offset potential Vofs) on a certain horizontal line.

[0190] However, this is not the essential drive condition, but the above-described interconnect structure is effective for suppressing shading and crosstalk even if the timing of potential change of the current supply line DSLb corresponding to another horizontal line does not overlap with the period of writing of the signal potential Vsig or the offset potential Vofs on a certain horizontal line.

(D-4) Drive System 4

[0191] In the above-described form examples, mobility correction is simultaneously executed in the period of writing of the signal potential Vsig.

[0192] However, the current supply line DSLb can also be applied to the case in which the writing of the signal potential Vsig and the mobility correction are carried out separately from each other.

(D-5) Drive System 5

[0193] In the above-described form examples, the current supply line driver 25 drives the current supply line DSLb from one side of the pixel array part 41.

[0194] However, the above-described interconnect structure can also be applied to the case in which one current supply line DSLb is driven from both the sides of the pixel array part 41.

[0195] In this case, the number of pixels driven by one current supply line driver 25 is half that when the current supply line DSLb is driven from one side.

[0196] Therefore, through calculation of the equation obtained by replacing the number of pixels N in Equation 1 by N/2, the voltage drop amount near the screen center can be obtained.

[0197] In this case, the line widths W3 and W4 are so designed as to provide such a resistance r per one pixel that the obtained voltage drop amount is not perceived as luminance difference.

(D-6) Pixel Structure 1

[0198] In the above-described form examples, the current supply line DSLb is applied to a top-emission pixel structure and therefore is particularly useful because there is no limit to the interconnect width.

[0199] However, the pixel structure is not necessarily limited to the top-emission structure but the current supply line DSLb can also be applied to a bottom-emission structure.

(D-7) Pixel Structure 2

[0200] In the above-described form examples, the pixel circuit includes two thin film transistors and the hold capacitor Cs.

[0201] However, the current supply line DSLb can also be applied to the pixel circuit including three or more thin film transistors. For example, the signal line DTL may be used exclusively for application of the signal potential Vsig, and an additional thin film transistor may be separately provided for application of the offset potential Vofs.

(D-8) Product Examples

(a) Electronic Apparatus

[0202] The above description has dealt with an organic EL panel as an example of an embodiment of the present invention. However, the above-described organic EL panel is also distributed in a commercial product form of being mounted to various kinds of electronic apparatus. Examples of products obtained by mounting the organic EL panel on electronic apparatus will be described below.

[0203] FIG. 34 shows a conceptual configuration example of electronic apparatus 51. The electronic apparatus 51 is composed of an organic EL panel 53, a system controller 55, and an operation input unit 57. As the organic EL panel 53, e.g. the organic EL panel 11 described for the second form example is used.

[0204] The details of processing executed by the system controller 55 differ depending on the commercial product form of the electronic apparatus 51. The operation input unit 57 is a device that accepts operation inputs to the system controller 55. As the operation input unit 57, e.g. a mechanical interface such as a switch or a button or a graphic interface is used.

[0205] The electronic apparatus 51 is not limited to apparatus of a specific field as long as it has a function to display an image and video produced therein or input from the external.

[0206] FIG. 35 is an appearance example of a television receiver as electronic apparatus to which the organic EL panel is applied.

[0207] On the front face of the casing of a television receiver 61, a display screen 67 composed of a front panel 63, a filter glass 65, and so on is disposed. The display screen 67 corresponds to the organic EL panel described for the form example.

[0208] Furthermore, e.g. a digital camera is available as this kind of electronic apparatus 51. FIGS. 36A and 36B show an appearance example of a digital camera 71. FIG. 36A shows an appearance example of the front-face side (imaging-subject side), and FIG. 36B shows an appearance example of the back-face side (photographer side).

[0209] The digital camera 71 includes a protective cover 73, an imaging lens unit 75, a display screen 77, a control switch 79, and a shutter button 81. The display screen 77 corresponds to the organic EL panel described for the form example.

[0210] Furthermore, e.g. a video camera is available as this kind of electronic apparatus 51. FIG. 37 shows an appearance example of a video camera 91.

[0211] The video camera 91 includes an imaging lens 95 that is disposed on the front side of a main body 93 and used to capture an image of a subject, a start/stop switch 97 for

imaging, and a display screen 99. The display screen 99 corresponds to the organic EL panel described for the form example.

[0212] Furthermore, e.g. a portable terminal device is available as this kind of electronic apparatus 51. FIG. 38 is an appearance example of a cellular phone 101 as the portable terminal device. The cellular phone 101 shown in FIGS. 38A and 38B are foldable type. FIG. 38A shows an appearance example of the casing-opened state, and FIG. 38B shows an appearance example of the casing-closed state.

[0213] The cellular phone 101 includes an upper casing 103, a lower casing 105, a connection (hinge, in this example) 107, a display screen 109, an auxiliary display screen 111, a picture light 113, and an imaging lens 115. The display screen 109 and the auxiliary display screen 111 correspond to the organic EL panel described for the form example.

[0214] Furthermore, e.g. a computer is available as this kind of electronic apparatus 51. FIG. 39 shows an appearance example of a notebook computer 121.

[0215] The notebook computer 121 includes a lower casing 123, an upper casing 125, a keyboard 127, and a display screen 129. The display screen 129 corresponds to the organic EL panel described for the form example.

[0216] Besides the above-described devices, an audio reproduction device, a game machine, an electronic book, an electronic dictionary, and so on are available as the electronic apparatus 51.

(D-9) Other Display Device Examples

[0217] The above description has dealt with the form examples applied to an organic EL panel.

[0218] However, the above-described drive technique can also be applied to other EL display devices. For example, the drive technique can also be applied to a display device including arranged LEDs and other display devices in which light-emitting elements having a diode structure are arranged on the screen. In addition, the drive technique can also be applied to a display device in which inorganic EL elements are arranged on the screen.

(D-10) Other Notes

[0219] Various modifications might be incorporated into the above-described form examples without departing from the scope of the present invention. In addition, various modifications and applications that are created or combined based on the description of the present specification are also available.

What is claimed is:

1. An electroluminescent display panel comprising:

a plurality of pixel circuits, at least one of the plurality of pixel circuits having a sampling transistor, a driving transistor, a capacitor, and an organic EL element;

a first potential wiring configured to supply a drive current, the first potential wiring having a first part and a second part; and

a second potential wiring configured to supply a signal potential, the second potential wiring including a first layer and a second layer, the second layer being disposed above the first layer,

wherein the sampling transistor is configured to supply the signal potential from the second potential wiring to the capacitor,

wherein the driving transistor is configured to supply the drive current from the first potential wiring to the organic EL element according to the signal potential,

wherein a first width of the first part of the first potential wiring that intersects with the second potential wiring is smaller than a second width of the second part of the first potential wiring that does not intersect with the second potential wiring, and

wherein the second potential wiring has a contact region connected between the first layer and the second layer.

2. The electroluminescent display panel according to claim 1, wherein the first potential wiring is arranged in the second layer.

3. The electroluminescent display panel according to claim 1, wherein a width of the first potential wiring is gradually increased from the first width to the second width.

4. The electroluminescent display panel according to claim 1, wherein the driving transistor is directly connected to the first potential wiring.

5. The electroluminescent display panel according to claim 1, wherein a width of the first potential wiring is changed in a stepwise manner between the first width and the second width.

6. The electroluminescent display panel according to claim 1, wherein the second potential wiring has a first metal formed in the first layer and a second metal formed in the second layer.

7. The electroluminescent display panel according to claim 1,

wherein the first potential wiring has a notch area corresponding to the first part, and

wherein the contact region of the second potential wiring is disposed in the notch area.

8. The electroluminescent display panel according to claim 1, wherein the drive current is configured to be supplied from both sides of one of the plurality of pixel circuits.

9. The electroluminescent display panel according to claim 1, wherein an interconnect resistance of the first layer is higher than an interconnect resistance of the second layer.

10. The electroluminescent display panel according to claim 1, wherein the electroluminescent display panel has a top-emission pixel structure.

11. An electroluminescent display panel comprising:

a plurality of pixel circuits, at least one of the plurality of pixel circuits having a sampling transistor, a driving transistor, a capacitor, and an organic EL element;

a first potential wiring configured to supply a drive current, the first potential wiring having a first part and a second part; and

a second potential wiring configured to supply a signal potential, the second potential wiring including a first portion formed in a first layer and a second portion formed in a second layer, the second layer being disposed above the first layer,

wherein the sampling transistor is configured to supply the signal potential from the second potential wiring to the capacitor,

wherein the driving transistor is configured to supply the drive current from the first potential wiring to the organic EL element according to the signal potential,

wherein a first width of the first part of the first potential wiring that intersects with the second potential wiring is

- smaller than a second width of the second part of the first potential wiring that does not intersect with the second potential wiring,
 wherein the first portion of the second potential wiring intersects with the first potential wiring,
 wherein the second portion of the second potential wiring is connected to the sampling transistor, and
 wherein the second potential wiring has a contact region connected between the first portion and the second portion.
12. The electroluminescent display panel according to claim 11, wherein the first potential wiring is arranged in the second layer.
13. The electroluminescent display panel according to claim 11, wherein a width of the first potential wiring is gradually increased from the first width to the second width.
14. The electroluminescent display panel according to claim 11, wherein the driving transistor is directly connected to the first potential wiring.
15. The electroluminescent display panel according to claim 11, wherein a width of the first potential wiring is changed in a stepwise manner between the first width and the second width.
16. The electroluminescent display panel according to claim 11, wherein the second potential wiring has a first metal formed in the first layer and a second metal formed in the second layer.
17. The electroluminescent display panel according to claim 11,
 wherein the first potential wiring has a notch area corresponding to the first part, and
 wherein the contact region of the second potential wiring is disposed in the notch area.
18. The electroluminescent display panel according to claim 11, wherein the drive current is configured to be supplied from both sides of one of the plurality of pixel circuits.
19. The electroluminescent display panel according to claim 11, wherein an interconnect resistance of the first layer is higher than an interconnect resistance of the second layer.
20. The electroluminescent display panel according to claim 11, wherein the electroluminescent display panel has a top-emission pixel structure.
21. The electroluminescent display panel according to claim 1, wherein a correction is executed when the sampling transistor is in a conductive state.
22. The electroluminescent display panel according to claim 1, wherein a correction is executed when the sampling transistor is supplying the signal potential from the second potential wiring.
23. An electronic apparatus comprising the electroluminescent display panel according to claim 1.
24. The electroluminescent display panel according to claim 11, wherein a correction is executed when the sampling transistor is in a conductive state.

25. The electroluminescent display panel according to claim 11, wherein a correction is executed when the sampling transistor is supplying the signal potential from the second potential wiring.

26. An electronic apparatus comprising the electroluminescent display panel according to claim 11.

27. An electroluminescent display panel comprising:

a plurality of pixel circuits, at least one of the plurality of pixel circuits having a sampling transistor, a driving transistor, a capacitor, and an organic EL element,
 a first potential wiring configured to supply a drive current, and
 a second potential wiring configured to supply a signal potential,

wherein a first width of a first part of the first potential wiring that intersects with the second potential wiring is smaller than a second width of a second part of the first potential wiring that does not intersect with the second potential wiring,

wherein the second potential wiring includes a first layer and a second layer which is upper than the first layer, and
 wherein the second potential wiring has a contact region connected between the first layer and the second layer.

28. An electroluminescent display panel comprising:

a plurality of pixel circuits, at least one of the plurality of pixel circuits having a sampling transistor, a driving transistor, a capacitor, and an organic EL element;

a first potential wiring configured to supply a drive current; and
 a second potential wiring configured to supply a signal potential,

wherein a first width of a first part of the first potential wiring that intersects with the second potential wiring is smaller than a second width of a second part of the first potential wiring that does not intersect with the second potential wiring,

wherein the second potential wiring includes a first portion formed in a first layer and a second portion formed in a second layer,

wherein the first portion of the second potential wiring intersects with the first potential wiring,

wherein the second portion of the second potential wiring is connected to the sampling transistor, and

wherein the second potential wiring has a contact region connected between the first portion and the second portion.

29. The electroluminescent display panel according to claim 27, wherein a correction is executed when the sampling transistor is supplying the signal potential from the second potential wiring.

30. The electroluminescent display panel according to claim 28, wherein a correction is executed when the sampling transistor is supplying the signal potential from the second potential wiring.

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摘要(译)

一种EL显示面板，具有对应于有源矩阵驱动系统的像素结构，EL显示面板包括电流供应线，该电流供应线被配置为共同连接多个像素电路，电流供应线的交叉部分的线宽信号线小于电流供应线另一部分的线宽。

